Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-10
MX10 Memory Multiplexor
Maintenance Manual

DEC-10-H1CA-D

MX10
MEMORY DATA MULTIPLEXOR MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION ▫ MAYNARD, MASSACHUSETTS

First Printing, May 1969

Instruction times, operating speeds and the like are included in this manual for reference only; they are not to be taken as specifications.

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The MX10 Memory Data Multiplexor, manufactured by Digital Equipment Corporation, is offered as an option for use in PDP-10 computer systems. Utilization of the MX10 allows the use of up to eight peripheral type processors, such as the DF10 Data Channel with the memory system.

The MX10 is normally installed in a DF10 Data Channel cabinet, where it occupies two logic panel locations. Figure 1-1 shows the front and back layouts of the MX10. There are no operating controls; all power is supplied and controlled by the associated DF10.

Granting of priorities for DF10 access to the multiplexor (thereby gaining access to a memory unit) is governed by logic contained within the MX10. Eight ports are provided for MPX control cables. In the event of simultaneous memory access requests, the processor whose control cable is terminated in the port designated P0 enjoys highest priority, while the processor associated with P7 has lowest priority of access.

A DF10 gains access to the multiplexor by sending a request signal over its MPX control cable. The multiplexor responds with an acknowledgment signal which enables the processor to gate out address information. Because of the necessity for this signal (required only in PDP-10 systems utilizing a multiplexor), arithmetical central processors of the KA10 type cannot be connected to the multiplexor bus.

After transmission of the acknowledgment signal over the MPX control line to the DF10 which has requested access, the MX10 "looks" exactly like the memory bus to the DF10 and the address information is transmitted directly to the memory unit over the MPX bus and the memory bus.

The MX10 logic contains a BUSY flag which precludes sampling of request signals while it is raised, thereby locking out any further requests while the multiplexor is being controlled by a specific channel. Other requests received simultaneously with that associated with the port granted access, remain true on the lines and are sampled for priority at the completion of the memory cycle in progress, when BUSY will be reset.

Detailed functional descriptions of the logic contained within the MX10 are presented in Chapter 5, Principles of Operation.

For information concerning the PDP-10 system see Section 1.3.

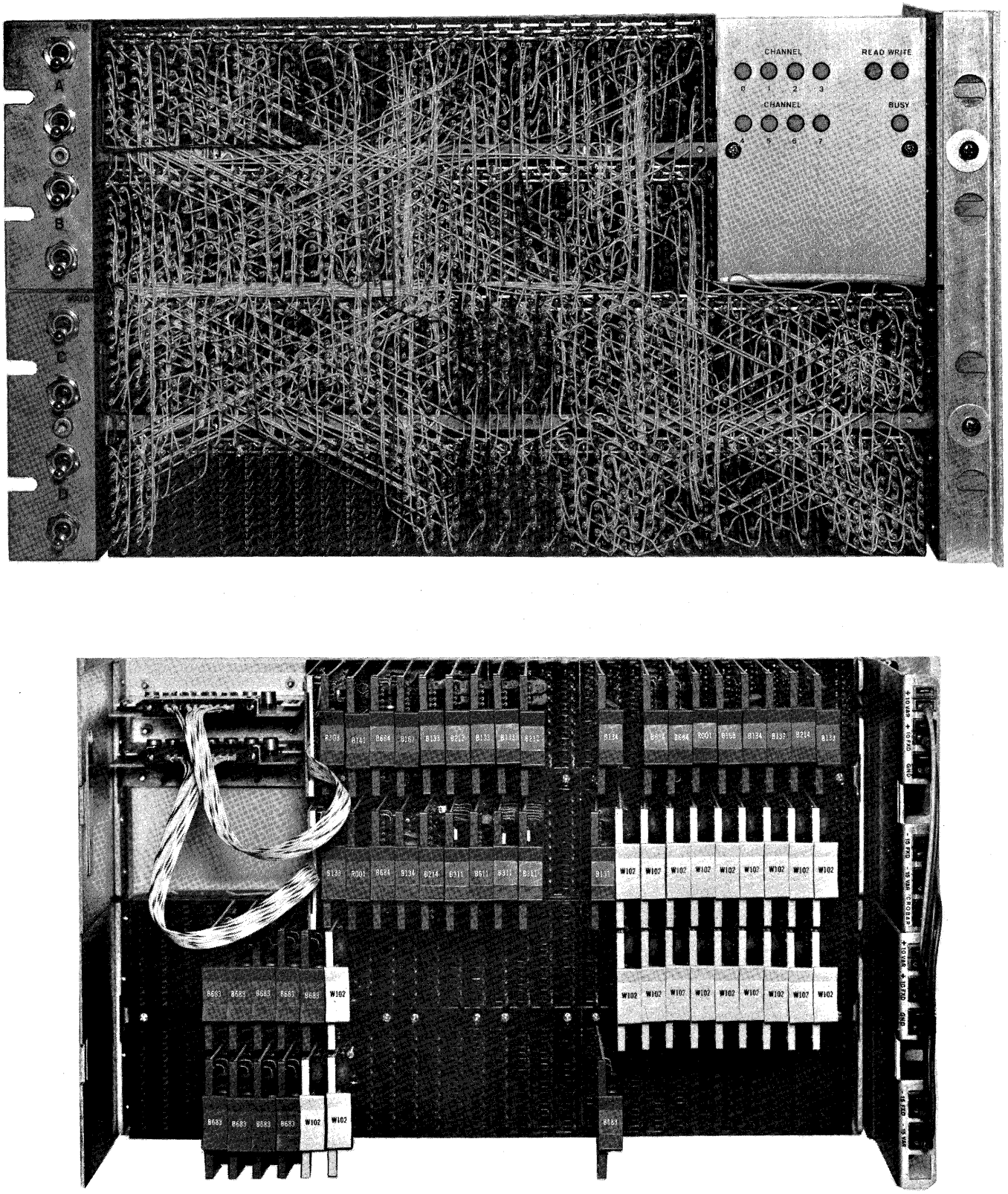


Figure 1-1 MX10 Front and Rear Views

1.2 SPECIFICATIONS

Power Requirements	+10V and -15V (furnished by the DF10)
Power Consumption	85W
Number of Ports	8
Size	Height 10-7/16 in. Depth 7-1/4 in. Width 19-1/8 in.
Delay	20 ns
Temperature	15.6°C to 37.8°C
Humidity	20% to 80%

1.3 REFERENCE MATERIAL

The documents listed in this section contain information essential to an understanding of the PDP-10 system and which, in some instances, supplements the material contained in this manual. These documents are available from Digital Equipment Corporation, 146 Main Street, Maynard, Massachusetts 01754 or from the nearest DEC District Office.

PDP-10 Interface Manual
PDP-10 System Reference Manual
MA10 - Core Memory, Maintenance Manual
DF10 - Data Channel, Maintenance Manual

CHAPTER 2
INSTALLATION

The MX10 is normally installed in place of the lower two blank panels in the DF10 Data Channel cabinet. All power is supplied and controlled by the DF10. Since the MX10 is installed in the DF10 cabinet, all installation requirements pertaining to site selection, environment, etc., are dictated by the DF10 and may be found in the PDP-10 Installation Manual.

2.1 INTERCONNECTIONS

Interconnection between the MX10 and DF10s is accomplished over the multiplexor bus which consists of two coaxial cable sets identical to the memory bus and a set of multiplexor control cables, one to each DF10, which carry the Request and Clear signals from a DF10 to the multiplexor and the Acknowledge signals in return. The multiplexor bus, like the memory bus, must be wired through each peripheral processor. Within each DF10, from incoming to outgoing connector, through sources and loads, twisted-pair wiring must be used. Each multiplexor control cable connects between a particular peripheral processor and the multiplexor and must terminate in 100Ω ±10% resistance at both ends.

The maximum length of the multiplexor bus is nominally 100 ft which includes the lengths of wire run through each memory and processor and a 30-ns delay (20 ft) through the MX10. Actual length of the bus is dependent upon the MX10's location in the system with respect to the memory unit and multiplexor bus. For additional information refer to Chapter 7 of the PDP-10 Interface Manual. Figure 2-1 is a block diagram of a hypothetical memory bus arrangement.

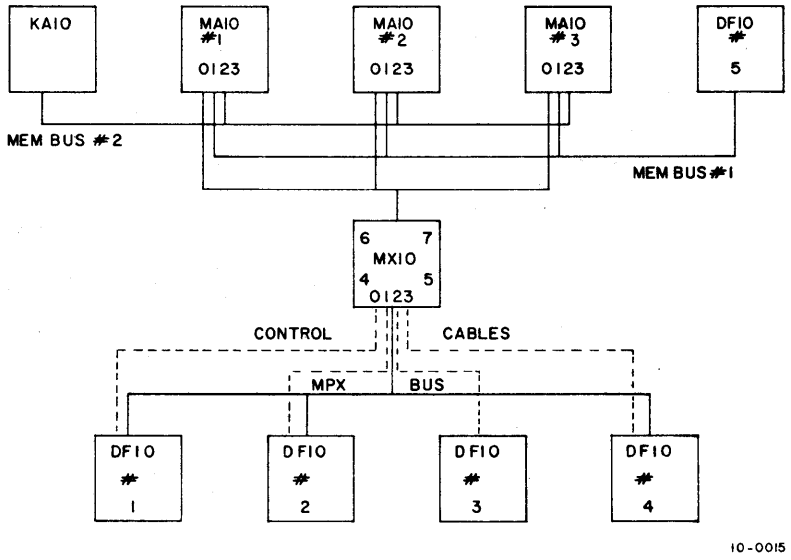
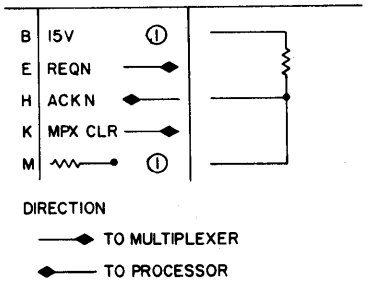


Figure 2-1 Hypothetical Memory Bus Arrangement

Pin assignments for the MPX control cable are illustrated in Table 2-1. Table 2-2 is a system interconnection diagram.

Table 2-1
Pin Assignments



Notes: Pins C, F, J, L, N, R, and V must be grounded.

① The -15V connection and the clamped load at pin M should be supplied at the processor end to facilitate operation of the processor without the multiplexer.

Table 2-2
Cable Interconnection Locations

Function	MX10		MA10		DF10	
	In	Out	In	Out	In	Out
MEMORY CABLE #2	A,B 13,14	A,B 1,2	S,T 19,20	S,T 17,18		
MEMORY CABLE #1	C,D 21,22	C,D 19,20	S,T 39,40	S,T 37,38		
MPX CABLE #2	C,D 1,2	C,D 13,14			K,L 1,2	K,L 9,10
MPX CABLE #1	C,D 29,30	C,D 31,32			E,F 1,2	E,F 31,32
MPX CONTROL*		P0 C15			L22	
		P1 C16			L22	
		P2 C17			L22	
		P3 C18			L22	
		P4 D15			L22	
		P5 D16			L22	
		P6 D17			L22	
		P7 D18			L22	

*One MPX Control Cable is required for each DF10 installed (maximum of eight).

CHAPTER 3
OPERATION

Operation of the MX10 is completely dependent upon the DF10 in which it is installed. The MX10 is provided with no controls of its own. Power potentials are provided to the MX10 logic when the associated DF10 is energized.

3.1 INDICATOR PANEL

Several indicator lamps are provided as shown in Figure 1-1. These indicators, which in normal operation change too rapidly to be meaningful, are provided as maintenance aids. The following table describes the meaning of a lamp when lit.

Indicator	Meaning
Channel 0 through 7	Indicates that the DF10 associated with a multiplexor port, 0 through 7, has requested control of the multiplexor and that one or more of the CHN storage flip-flops are set.
READ	Indicates that the multiplexor is in the READ mode and that RDWR1 and RDWR2 are in their 0 states.
WRITE	Indicates that the multiplexor is in the WRITE mode and that RDWR1 and RDWR2 are in their 1 states.
BUSY	Indicates that a memory cycle is in progress. This lamp is lighted by BUSY DY (1) and extinguished by FIN DY.

CHAPTER 4
PRINCIPLES OF OPERATION

This section describes the operations which take place within the MX10 logic during Power Up, Request, Read, Write, and Read-Modify-Write conditions. Reference is made to the noun titles of the Engineering Drawings contained in Chapter 7 of this manual. Locations given refer to the Engineering Drawings and not to MX10 logic panels.

4.1 POWER-ON CONDITION

This discussion refers to Sheet 2 of the Control drawings. The delay associated with the R303 One Shot at location 7B is adjusted so that it exceeds the time required for the +10V and -15V potentials to reach 90% of their final values at power turn-on; this condition causes the multivibrator to go initially to its 1 state. Upon expiration of the 1-s delay, the positive-going transition of the output level is applied to the input of a B611 Pulse Amplifier whose output is inverted through a B611 NAND gate. This positive pulse, designated CLEAR, is applied to another B611 Power Amplifier at location 4D where the FIN pulse is generated, and, after further amplification and a 65-ns delay associated with the B311 also at location 4D, positive and negative FIN DY pulses are developed. In location 3D, the positive assertion of FIN DY resets BUSY (the B212 in location 3D) whose 0 state causes the B212 at location 2D (BUSY DY) to be cleared also.

Generation of these pulses causes the MX10 to be placed in a ready condition wherein it can respond to memory access requests from a processor. The BUSY flag has been lowered indicating that a memory cycle is not in progress, while the same pulse which caused clearing of BUSY, FIN DY also direct sets the B212 flip-flops, RDWR1 and RDWR2 (location 3-4B). The RDWR1(1) and RDWR2(1) levels are the qualifying conditions for enabling the gates associated with the data transceivers (sheet 1 of the Data Transceiver drawings) which will allow transfers of data from the multiplexor bus to the memory bus.

FIN (which was generated 65 ns before FIN DY), referring to sheet 1 of the Control drawings, causes each of the eight B214 Request Storage flip-flops, in locations 2B-7B, to be direct cleared.

4.2 REQUEST OPERATIONS

A processor requesting access to the memory system will place a negative level on its REQ control line.

The REQ N level or levels, if more than one processor is simultaneously requesting access, are NANDed in eight identical B133 gates in the Control logic (sheet 1, locations 2B to 8B) where at each gate BUSY (0), the remaining level required for enabling becomes true during the Power-On

phase. The positive levels of the enabled gates will collector set the associated B214 flip-flops (CHN0 through CHN7). It is therefore possible to load more than one of the eight CHN request storage flip-flops during the time BUSY (0). BUSY is set through its delayed-set input by any REQ N ANDed with BUSY (0) at the B133 and B141 gates (located at 3C of sheet 2 of the Control drawing). Because of this, the MX10 logic must now assign priorities to each of the eight access ports to preclude more than one processor from gaining access to memory. Priorities are assigned in descending order from 0 to 7, where the processor associated with port 0 enjoys highest priority.

Across the top of the Control drawing sheet 1 are eight bus drivers, each with its associated gated input circuitry. Negative assertion of the PRCRBR level from the processor must be present at each R001 gate to allow an output from any of the bus drivers. ACK N levels therefore will not be placed on the MPX lines while the processor is in an abnormal power condition. The following discussion will proceed on the assumption that PRCRBR is negatively asserted.

The only condition for the generation of ACK 0 is CHN 0 (1) and BUSY DY (1) asserted at the B134 AND gate at location 7D. BUSY DY (1) is set by BUSY DY (0) which is ANDed with BUSY (1) in a B133 gate (at location 1D of sheet 2 of the Control drawing).

If CHN 1 (1) is true simultaneously with the CHN 0 (1) condition, and examination of the input gating associated with the generation of ACK 1 (the B134 and B167 gates at 7C of sheet 1 of the Control drawing), shows that a condition for enabling the B167 AND gate is CHN 0 (0), ACK 1 can never be generated if CHN 0 (1) is true. First priority has been assigned by the logic to the processor associated with P0. Each of the remaining six gates are disqualified by assertion of a CHN (1) of lower designation in the same manner that generation of ACK 1 was inhibited by the assertion of CHN 0 (1). In one instance, for simplification, a HI ACK level is generated in a B137 AND gate at 4C. This level, dependent upon the CHN 0 through 3 (0) condition, is an enabling requirement for generation of ACK 4 through ACK 7.

4.3 MEMORY READ CYCLE

The ACK level associated with the processor having control is placed on the appropriate MPX control line. The DF10 now responds with a REQX CYC signal and the memory address word including the type of request (i.e., Read, Write or Read-Modify-Write) over the MPX bus which terminates in the B683 Bus Drivers (as illustrated on the Bus Drivers and Control drawing). These levels exit the bus drivers over the memory bus to the memory system, where a particular memory unit will be selected.

When a memory unit has allowed access, it brings up ADDR ACK on an MAI line which is applied to a W102 Bus Driver (at location 2B of the Bus Drivers and Control drawing). This pulse exits the bus driver over the multiplexor bus to the DF10 as ADDRACKX.

This is to be a READ operation, therefore MCRD is asserted and ANDed with ADDRACK (at a B133 gate at location 5B of sheet 2 of the Control drawing) which resets the RDWR1 and RDWR2 flip-flops.

The memory now simultaneously asserts RDRS, through a bus driver (location B2 of the bus drivers and control logic), and places the data from the addressed memory location (36 bits) on the memory bus. RDRSX at this time also clears CHN 0 through 7 in the same manner as the assertion of FIN during Power-On.

Since RDWR1 and RDWR2 are both in the 0 state (refer to the Data Transceiver Drawing), one condition required for enabling the input gate associated with each W102 Bus Driver has been fulfilled. The remaining condition is the state (0 or 1) of each bit in the addressed memory location as it is strobed into the memory buffer. All 1s placed on the memory bus enable the gates and bring up the MPX lines associated with the bit. In this manner the selected data is read into the DF10 over the MPX bus.

This completes the memory cycle for the multiplexor and the data channel, although additional operations are necessary within the addressed memory unit before it is again ready for access. The MX10 must now prepare to receive and process the next request to be made.

On the Control drawing (Sheet 1, location 6C), it is shown that the assertion of RDRS causes generation of RDRS DY after completion of the 65-ns delay associated with the B311 Delay Line. RDRS DY ANDed with WR BUF (0) (true when ADDRACK and ~MCWR are asserted) produces CLEAR which, in turn, sets up the MX10 for the next cycle request in the same manner as previously described in Section 4.1.

4.4 MEMORY WRITE OPERATION

Prior to commencement of the WRITE operation, the MX10 must be in the ready condition as at the termination of READ or Power Up. Selection of a DF10 through the priority logic takes place as described in Section 4.2.

The memory address word is accompanied by a WRITE RQ level (MXCWR on the MPX bus and MCWR on the memory bus). This level is transmitted through a B683 Bus Driver at location 6C of the Bus Drivers and Control drawing. MCWR causes generation of ~MCWR at a B133 gate shown on sheet 2 of the Control drawing where, in location 6B, ~MCWR causes the WR BUF (1) condition. ADDRACKX ANDed with MCWR in the control logic clears CHN 0 through 7.

RDWR1 and RDWR2 are on 1s, since they were set by FIN DY 65-ns after the last CLEAR. This is the condition required in the data transceiver (sheet 1) for transfer of data from the multiplexor bus to the memory bus.

At generation of ADDRACK, a memory unit has been selected, has acknowledged the receipt of a legal address, and is awaiting data and a write restart (WRRS) pulse.

The DF10 upon receipt of ADDRACK, generates WRRS and simultaneously places the data to be written on the multiplexor bus where it is transmitted through the bus drivers, onto the memory bus, and into the memory unit's buffer.

Assertion of WRRS, after a 65-ns delay, generates WRRS DY and CLEAR in the control logic; once again readying the MX10 for the next memory cycle.

4.5 READ-MODIFY-WRITE

Operation during the READ-MODIFY-WRITE cycle is similar to that for a READ or WRITE except that the CLEAR pulse is inhibited following the READ portion of the cycle, thereby preventing the MX10 from disconnecting, and lowering the BUSY flag.

Since both MCRD and MCWR are asserted for the READ-MODIFY-WRITE cycle, WR BUF (1) is generated by ADDRACK which clears RDWR1 and RDWR2 (MCRD being true). The READ portion of the cycle progresses as before, due to the states of RDWR1 and RDWR2. CLEAR is not generated by RDRS DY at the completion of the READ cycle because of the WR BUF (0) inhibiting level at the B311 gate (located at 5C of sheet 1 of the Control drawing). RDRS DY sets RDWR1 and RDWR2 to their WRITE state. The multiplexor therefore remains connected until a WRRS is asserted by the DF10 and data is placed on the multiplexor bus for writing as in a normal WRITE cycle. The cycle then continues as described in Section 4.4.

4.6 NONEXISTENT MEMORY OPERATION

When a nonexistent memory situation is detected by the processor, the processor places a clear signal CLR 0-7 on the MPX control cable with which it is associated. These pulses are ORed together in the control logic and cause generation of CLEAR within the logic, causing the disconnection of the MX10 from the processor and a return to the ready condition.

CHAPTER 5
MAINTENANCE

General preventive and corrective maintenance procedures for the MX10 are contained in the Maintenance Section, Chapter 4 of the DF10 Data Channel maintenance manual. Specific test procedures are completely dependent upon and integrated with those for the DF10 except for those contained in Section 5.3.

5.1 TEST PROCEDURE (DISK)

The following equipment configuration is required for accomplishment of the Disk Test procedure:

DF10	Data Channel
MX10	Multiplexor (installed in DF10 cabinet)
RC10	Synchronizer
RD10	Disk

With the MX10 installed in the above configuration, accomplishment of the "Disk System Acceptance Test Procedure and Specifications", drawing A-SP-RC10-0-9, will constitute the acceptance test for the MX10.

5.2 TEST PROCEDURE (OFF-LINE)

Accomplishment of this test procedure requires that the MX10 be installed within the DF10 cabinet with the MPX bus and control cables connected. The DF10 (off-line) test, drawing DF-10-0-7, will be run with the following additional steps.

a. Remove the W990 module from location L22 of the DF10.

b. The channel tester is connected to the DF10 via the channel bus and to the MX10 via the memory bus.

c. The MPX control cable is connected to port 0 in the MX10.

d. During step A,2 of the DF10 Off-Line Control test, verify that RDRS delay time (defined as RDRS to FIN) is within the limits of 85 ns ± 6 ns and that the FIN delay time (defined as FIN to FIN DY) is within the limits of 76 ns ± 5 ns.

e. Sync (-) on REQ 0 and verify that BUSY, CHN 0, and ACK 0 go true at this time. Also, verify that FIN DY clears BUSY.

f. Relocate the MPX control cable to port 1 and repeat (e) above. Continue to shift the control cable and repeat (e) until all ports have been checked.

g. During accomplishment of steps 2 and 4 of the DF10 Data Test, the total cycle time will be increased by two multiplexor delays or 40 ns.

h. Also during step 4 of the DF10 Data Test, with WRITE on a 1, verify the WRRS delay time (defined as WRRS to FIN) which should be within the limits of 85 ns ± 6 ns.

i. During step A,5 of the DF10 Termination Test, with NO MEM on a 1, verify that CLRN clears BUSY. This procedure should be repeated for the remaining seven ports.

5.3 TEST PROCEDURE (Using MX10T OFF LINE TESTER)

5.3.1 General

Off-line test procedures may also be carried out using the MX10T Off-Line Tester. This procedure has an additional advantage in that it may be used in special systems where no DF10 is installed and the DF10 Diagnostic Programs are not applicable.

Within the MX10T, circuitry is provided to initiate REQ N on any two multiplexor ports and to confirm that an ACK N from only the higher priority port is generated in response. Other conditions such as: no ACK; ACK from a lower priority port; or ACK always true, result in an error indication. The MX10T also generates the following signals necessary to cycle the MX10 for trouble-shooting purposes in simulated memory READ, WRITE, and READ-MODIFY-WRITE cycles:

ADDRACK
RDRS
WRRSX
MCXRD
MCXWR

5.3.2 Test Configuration

The MX10T is mounted in the same cabinet as the MX10 and is connected as shown in Figure 5-1. Test cables must not be connected while the MX10 is running on-line.

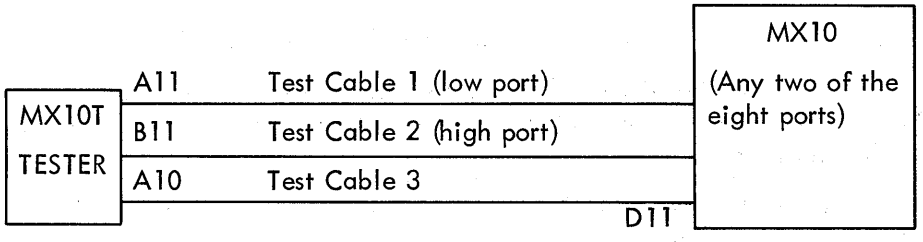


Figure 5-1 Test Configuration (MX10T Off Line)

5.3.3 Priority Network Check

a. Connect test cables 1 and 2 to the ports selected to be checked. Test cable 1 connects to the lower numbered port (higher priority).

b. Turn the READ and WRITE switches OFF and the TEST MODE switch ON.

c. Cycle the tester by pressing the START button. This causes REQ N to be transmitted to both ports. Only ACK from the port with lowest priority should be asserted by the MX10. If no ACK is generated, or if an ACK from the port associated with the higher priority is sensed, ERROR will set. Upon completion of the priority checks, the MX10 is cleared by CLR N. ERROR will also set if ACK N fails to go false after the CLEAR.

d. The tester recycles automatically but will stop if ERROR sets and the ERROR STOP switch is ON. In this case, the MX10 is not cleared.

5.3.4 Memory Cycle Simulation

This procedure is used to cycle the MX10 for troubleshooting purposes.

a. Connections are as shown in Figure 5-1.

b. Set the READ and WRITE switches for the type of simulated memory cycle desired:

READ = 1	READ Cycle
WRITE = 1	WRITE Cycle
READ = 1 and WRITE = 1	READ-MODIFY-WRITE Cycle

Put the TEST MODE switch ON.

c. Cycle the tester by pressing the START button. A priority network check is made as in Section 5.3.3, except that CLR N is not generated. The priority network check is followed by generation of the appropriate memory and MPX bus signals over test cable 3 simulating the selected memory cycle type. The following are the signals generated for the various switch settings:

READ	ADDRACK, RDRS
WRITE	ADDRACK, WRRSX
READ, WRITE	ADDRACK, RDRS, WRRSX

d. ERROR will set in the event of a priority network failure or if the MX10 fails to clear during a tester cycle.

5.4 MARGIN TESTS

The frequency of voltage margin testing is dependent upon conditions at the site; monthly testing is suggested. These tests are accomplished while the Diagnostic Program, 5CA FLOAT, is in progress. Table 5-1 lists the voltage margin specifications. The second figure shown for Panels A and B, under +10V Low, is due to the B684 Bus Drivers and will be true for Panel A when ports 0, 1, 4, 5, 6, or 7 are used and for Panel B when ports 2 or 3 are used.

Table 5-1
Voltage Margin Specifications

Mounting Panel	+10V		-15V	
	Low	High	Low	High
A	2.5 (5.5)	17.5	-18	-12
B	2.5 (5.5)	17.5	-18	-12
C	2.5	17.5	-18	-12
D	2.5	17.5	-18	-12

CHAPTER 6
SPARE PARTS

This section contains a listing of the modules used in the MX10 with suggested quantities of each type to be stocked by the user at his site.

Table 6-1
Spare Parts

DEC Type Number	Description	Recommended Spare Quantity
	MODULES	
B133	Diode Gate	1
B134	Diode Gate	1
B137	Diode Gate	1
B141	Diode Gate	1
B167	Adder Gate	1
B168	Diode Gate	1
B212	Flip-Flop	1
B214	Quadruple Flip-Flop	1
B311	Delay Line	1
B611	Pulse Amplifier	1
B683	Bus Driver	2
B684	Bus Driver	1
R001	Diode Network	1
R303	Integrating One Shot	1
W102	Bus Driver	1
	TRANSISTORS	
15-03099	DEC 2894-3B-S	4
15-01742	2N2904	4
15-03100	DEC 3009B-S	2
15-02151	2N3605	2

Table 6-1 (Cont)
Spare Parts

DEC Type Number	Description	Recommended Spare Quantity
15-02762-02	DEC 3639-D	2
15-05321	2N4258	4
	DIODES	
11-00113	D662	10
11-00114	D664	10
11-02161	D668	6
	MISCELLANEOUS	
12-02116	Indicator Lamps	10

CHAPTER 7
ENGINEERING DRAWINGS

This chapter contains reduced copies of DEC block schematics, circuit schematics, and other engineering drawings necessary for understanding and maintaining this equipment. Only those drawings which are essential or are not available in the referenced pertinent documents are included. Should any discrepancy exist between the drawings in this chapter and those supplied with the equipment, assume that the latter drawings are correct.

7.1 DRAWING TERMINOLOGY

7.1.1 Drawing Numbers

DEC engineering drawing numbers contain five groups of information, separated by hyphens. A drawing number such as BS-D-9999-1-5 consists of the following information reading from left to right: a 2- or 3-letter code specifying the type of drawing (BS); a 1-letter code specifying the size of the original drawing (D); the type number of the equipment (9999); the manufacturing series of the equipment (1); and the drawing number within a particular series (5). The drawing type codes are:

BS, block schematic or logic diagram
CD, cable diagram
CL, cable list
CS, circuit schematic
FD, flow diagram
PW, power wiring
RS, replacement schematic
UML, utilization module list
WD, wiring diagram
WL, wiring list

7.1.2 Circuit Symbols

Block schematic engineering drawings of DEC equipment indicate signal flow, logical functions, circuit type and physical location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using symbols that define the circuit operation. These symbols are similar to those appearing in both the FLIP CHIP Modules Catalog and the System Modules Catalog but are often simplified. Figure 7-1 illustrates some of the symbols used in DEC engineering drawings.

7.1.3 Logic Signal Symbols

DEC standard logic signal symbols are shown at the input of most circuits to specify the enabling conditions required to produce a desired output. These symbols represent either standard DEC logic levels, standard DEC pulses, standard FLIP CHIP pulses, or level transitions.

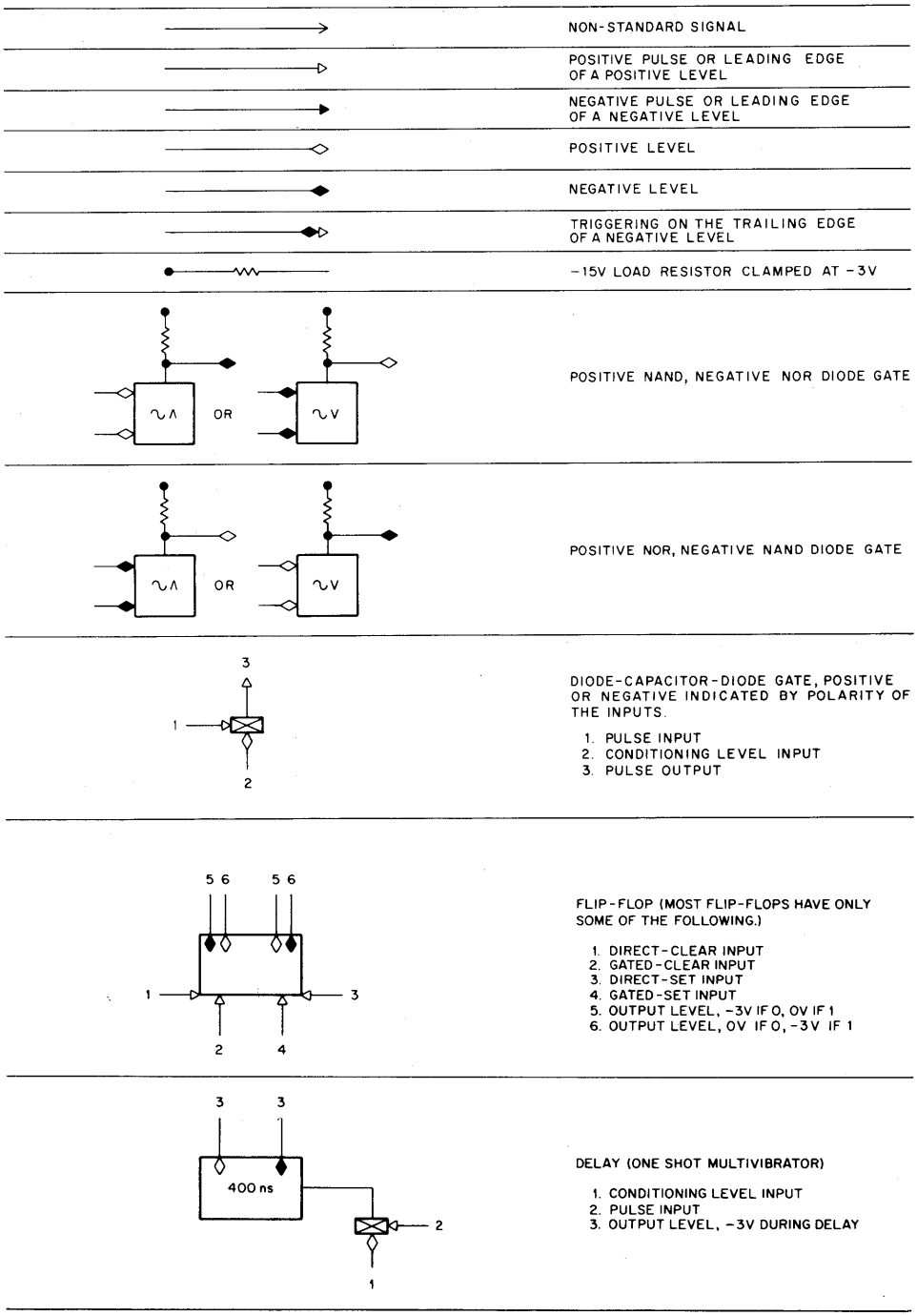


Figure 7-1 DEC Symbols

7.1.4 Logic Levels

The standard DEC logic level is either at ground (0 to -0.3V) or at -3V (-2.5 to -3.5V). Logic signals generally have mnemonic names which indicate the assertion condition of the signal. An open diamond (—◇) indicates that the signal is a DEC logic level and that ground represents assertion; a solid diamond (—◆) indicates that the signal is also a DEC logic level and that -3V represents assertion. All logic signals at the conditioning level inputs of diode-capacitor-diode gates must be present for a specified length of time (depending on the module used) before an input pulse will trigger operation of the gate.

7.1.5 Standard Pulses

DEC standard pulses are 2.5V in amplitude with reference to either ground or -3V, depending upon the type of module used. The width of a standard pulse is either 40, 70, or 400 ns as required for specific circuit configurations. The standard 2.5V negative pulse (-2.3 to -3.5V) is indicated by a solid triangle (—▶) and is always referenced with respect to ground, as shown in Figure 7-2.

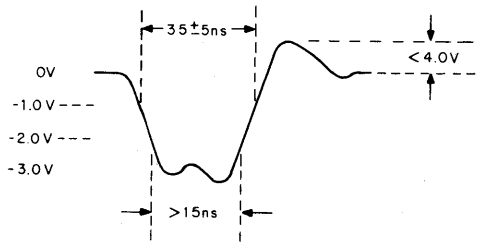


Figure 7-2 Standard Negative Pulse

The standard positive pulse is the inverse of the negative pulse and is indicated by an open triangle (—▷). The positive pulse goes either from -3V to ground or goes from ground to +2.5V (+2.3 to +3.0V).

7.1.6 FLIP CHIP Standard Pulses

FLIP CHIP circuit operation utilizes two types of pulses, R- and S-series, and B-series. The pulse produced by R- and S-series modules starts at -3V, goes to ground (-0.2V) for 100 ns, then returns to -3V. This pulse is shown in Figure 7-3.

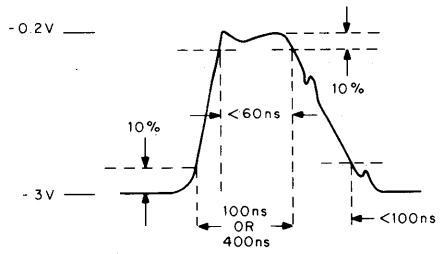


Figure 7-3 FLIP CHIP R- and S-Series Pulses

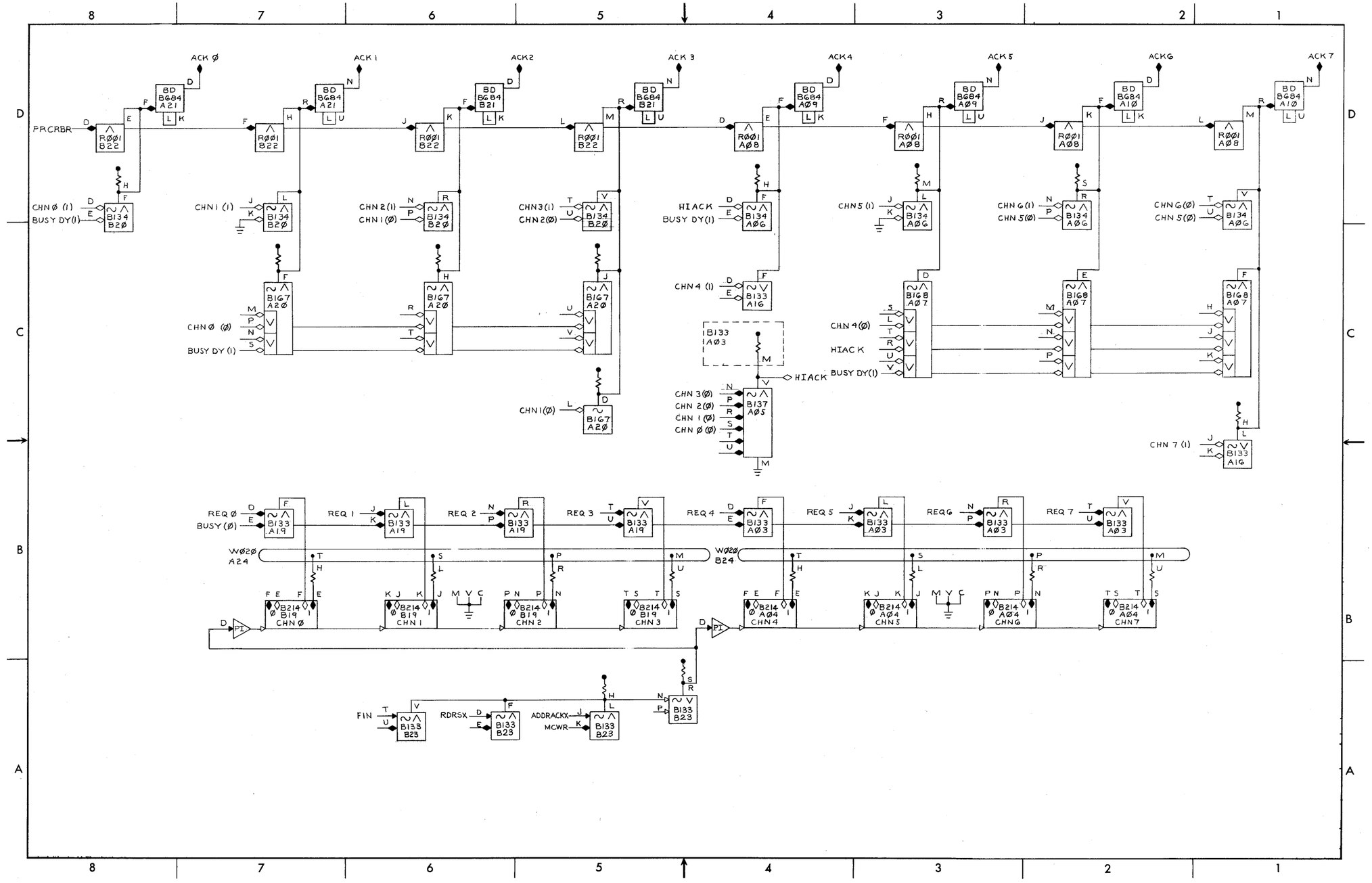
The B-series negative pulse is 2.5V in amplitude and 40 ns in duration and is similar to the one shown in Figure 7-2. If this pulse arrives at the base of an inverter, the inverter output will be a narrow pulse, similar in shape to the R-series standard pulse. The B-series positive pulse, which goes from ground to +2.5V, is the inverse of the B-series negative pulse.

7.1.7 Level Transitions

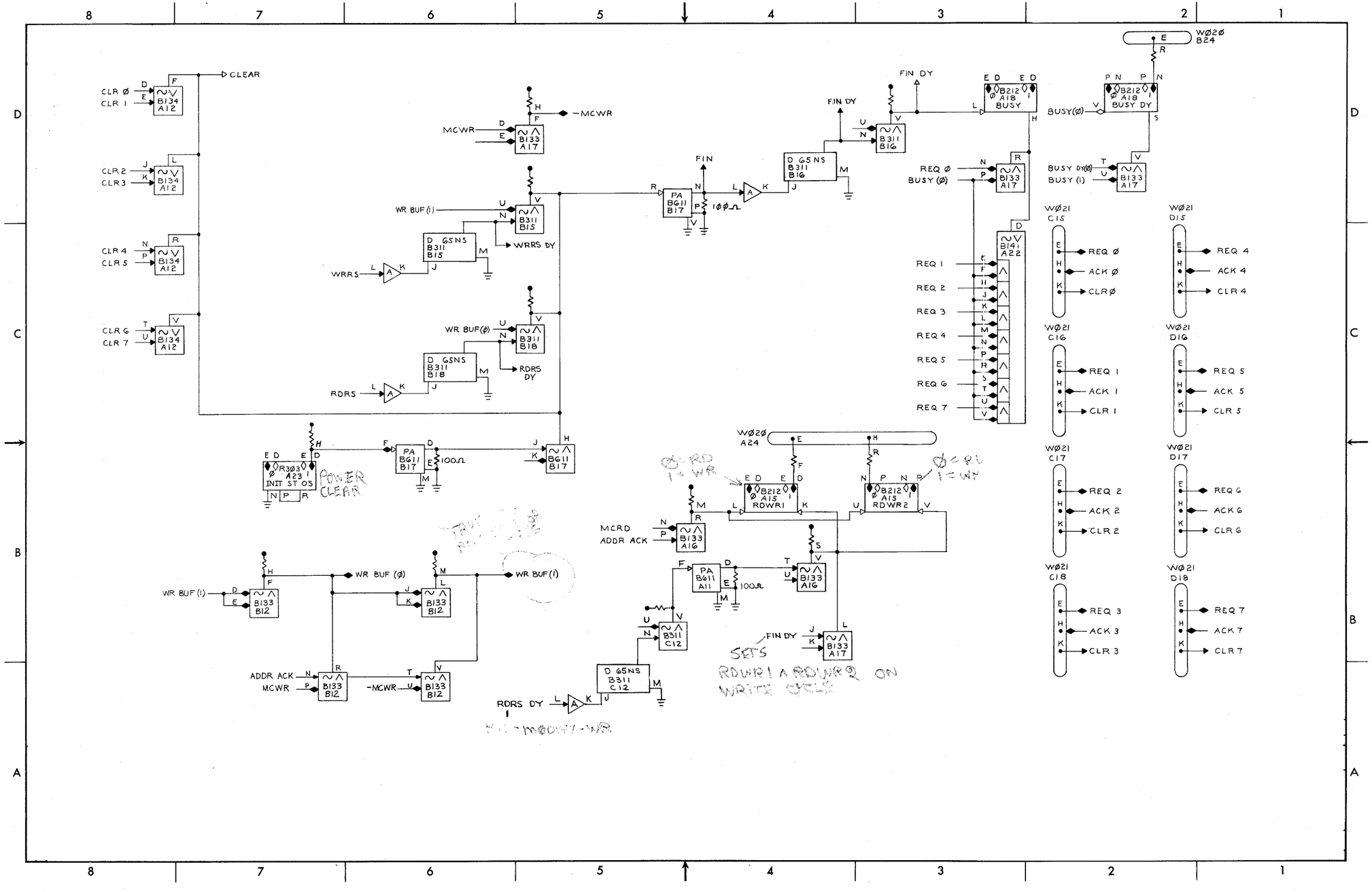
Occasionally, the transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (—◆▷) indicates this fact. The triangle is drawn open or solid depending, respectively, on whether the positive (-3V to ground) or the negative (ground to -3V) transition triggers circuit action. The shading of the diamond either is the same as that of the triangle to indicate triggering on the leading edge of a level or is opposite that of the triangle to indicate triggering on the trailing edge. An arrowhead (——>) pointing in the direction of signal flow indicates nonstandard signals (power supply outputs, analog signals, etc.).

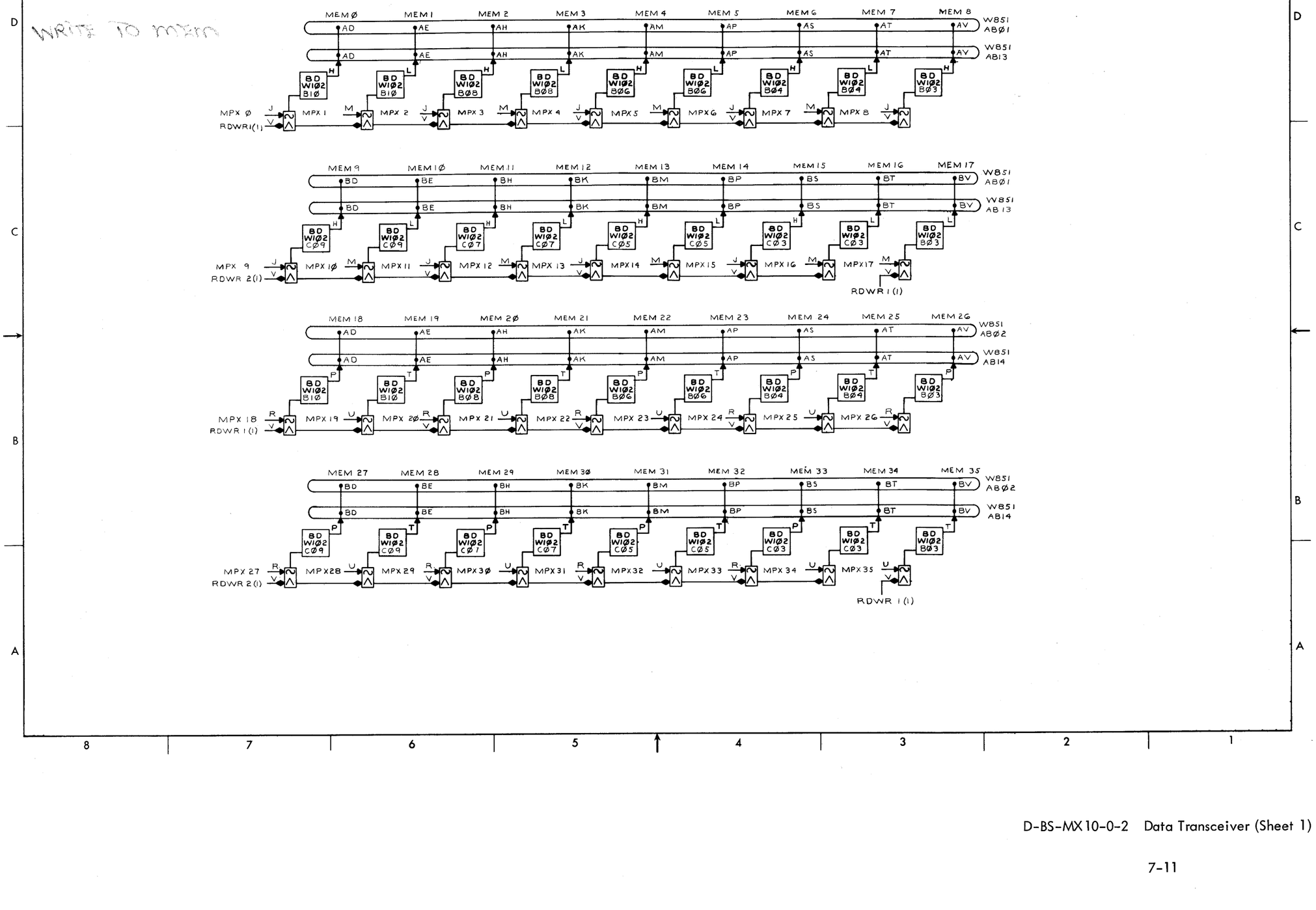
7.2 MX10 DRAWINGS

Drawing No.	Title	Rev.	Page
D-BS-MX10-0-1	Control (2 Sheets)	B	7-7
D-BS-MX10-0-2	Data Transceiver (2 Sheets)	--	7-11
D-BS-MX10-0-3	Bus Drivers and Control	B	7-15
D-BD-MX10-0-4	Master Block Diagram	--	7-17
D-FD-MX10-0-5	Flow Chart and Diagram	B	7-19
D-MU-MX10-0-6	Module Utilization	C	7-21
C-AD-7005509-0-0	Wired Assembly	--	7-23
B-CS-B133-0-1	Diode Gate	B	7-24

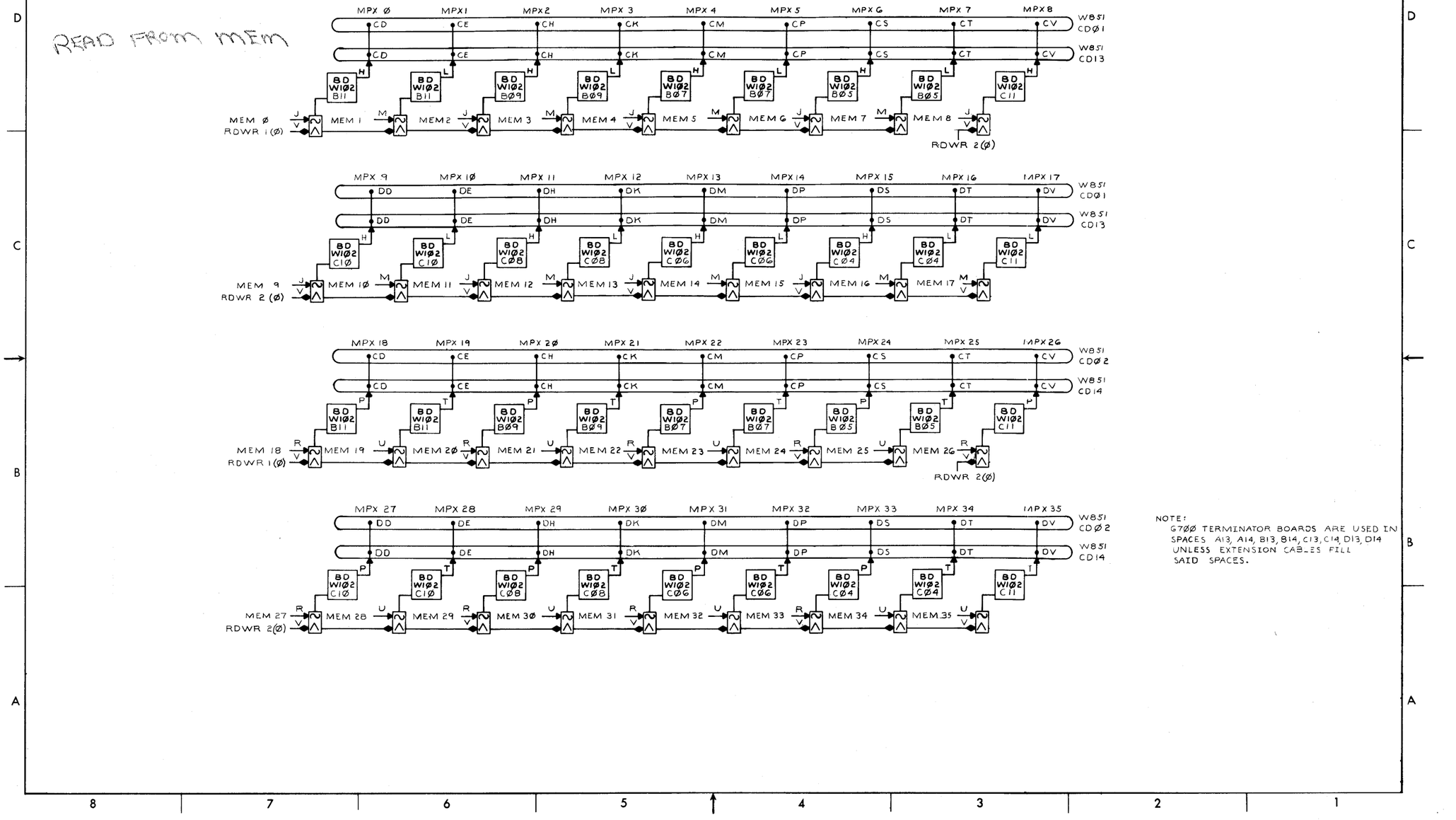


D-BS-MX10-0-1 Control (Sheet 1)

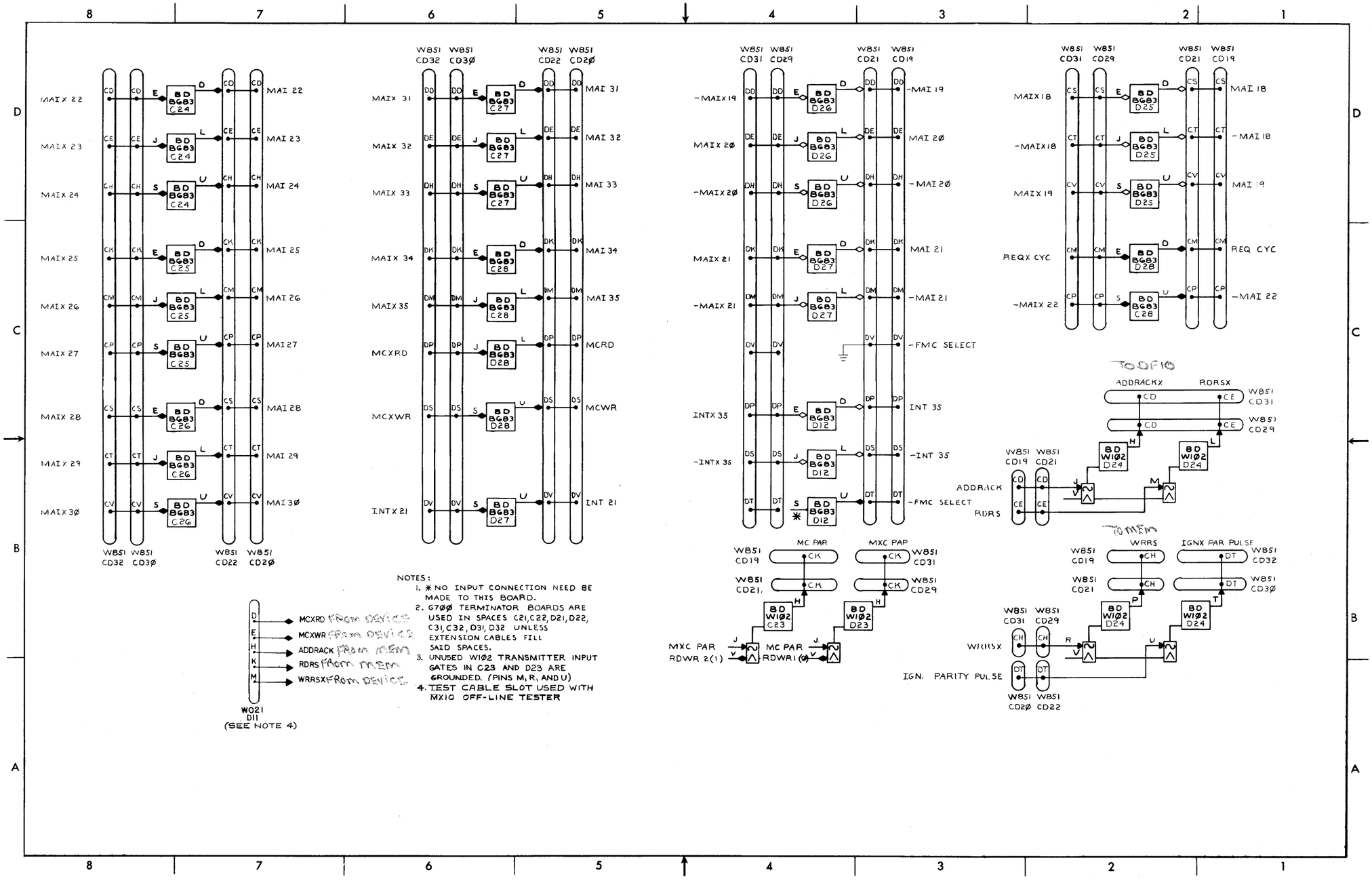

CLEAR
CLR Ø
CLR 1
CLR 2
CLR 3
CLR 4
CLR 5
CLR 6
CLR 7
B134 A12
MCWR
B133 A17
WR BUF (1)
WRRS DY
WRRS
RDRS DY
RDRS
B311 B15
B311 B18
D GSNS B311 B15
D GSNS B311 B18
PA B611 B17
100Ω
B611 B17
R303 Ø A23 1 INIT ST 05
POWER CLEAR
FIN
FIN DY
D GSNS B311 B16
B311 B16
REQ Ø
BUSY (Ø)
B133 A17
B212 Ø A18 BUSY
B212 Ø A18 BUSY DY
BUSY (1)
WØ2Ø B24
B141 A22
REQ 1
REQ 2
REQ 3
REQ 4
REQ 5
REQ 6
REQ 7
WØ21 C15
WØ21 D15
REQ Ø
ACK Ø
CLR Ø
REQ 4
ACK 4
CLR 4
WØ21 C16
WØ21 D16
REQ 1
ACK 1
CLR 1
REQ 5
ACK 5
CLR 5
WØ21 C17
WØ21 D17
REQ 2
ACK 2
CLR 2
REQ 6
ACK 6
CLR 6
WØ21 C18
WØ21 D18
REQ 3
ACK 3
CLR 3
REQ 7
ACK 7
CLR 7
WØ2Ø A24
B212 Ø A15 RDWR1
B212 Ø A15 RDWR2
MCRD
ADDR ACK
B133 A16
B311 C12
D 6SNS B311 C12
B611 A11
B133 A16
FIN DY
B133 A17
SETS RDWR1 & RDWR2 ON WRITE CYCLE
WR BUF (1)
WR BUF (Ø)
B133 B12
ADDR ACK
MCWR
-MCWR
RDRS DY

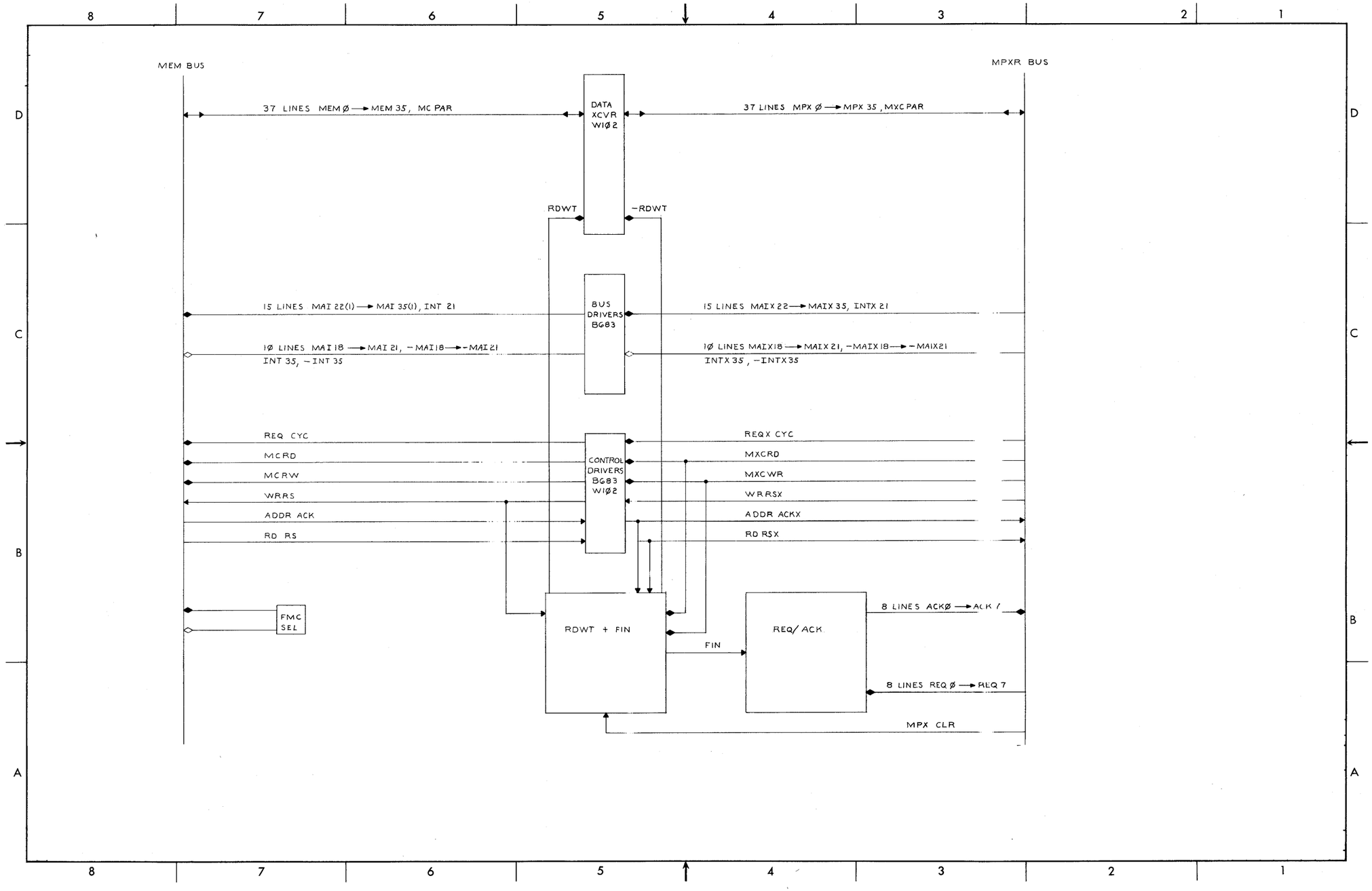


D-BS-MX10-0-2 Data Transceiver (Sheet 1)

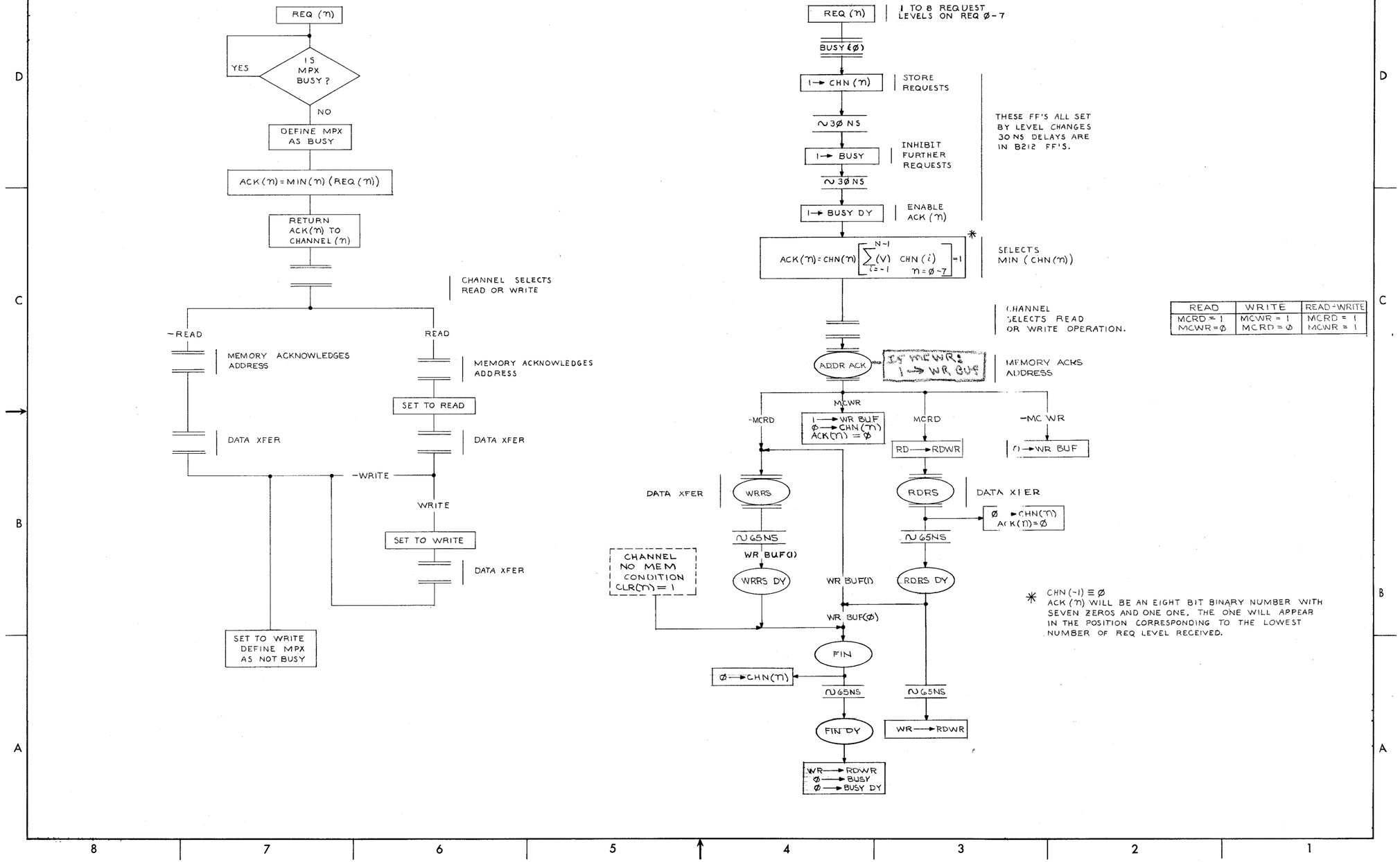


D-BS-MX10-0-2 Data Transceiver (Sheet 2)

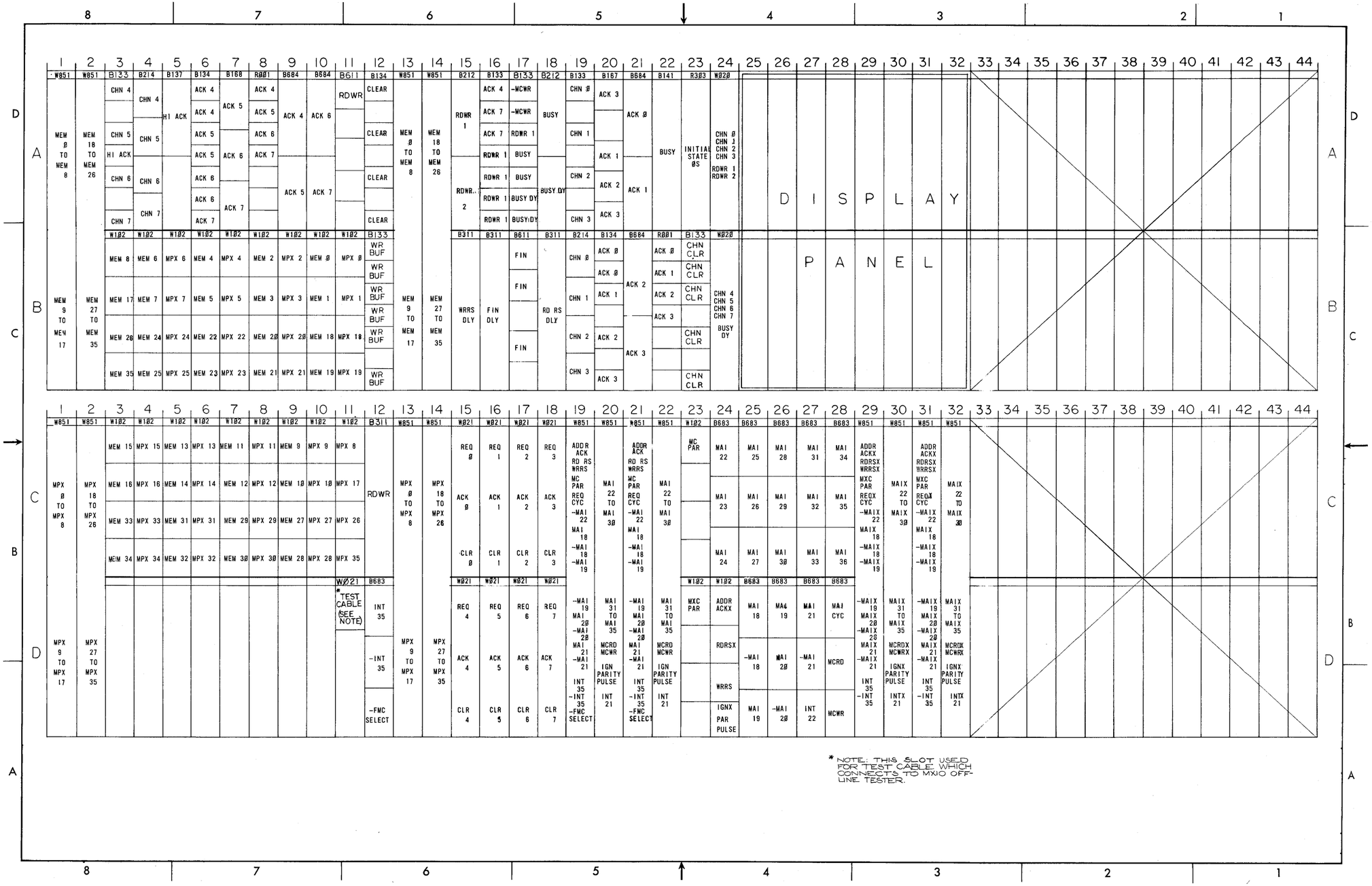

8
7
6
5
4
3
2
1
D
C
B
A
MAIX 22
MAIX 23
MAIX 24
MAIX 25
MAIX 26
MAIX 27
MAIX 28
MAIX 29
MAIX 30
MAI 22
MAI 23
MAI 24
MAI 25
MAI 26
MAI 27
MAI 28
MAI 29
MAI 30
W851 CD32
W851 CD30
W851 CD22
W851 CD20
MAIX 31
MAIX 32
MAIX 33
MAIX 34
MAIX 35
MCXRD
MCXWR
INTX 21
MAI 31
MAI 32
MAI 33
MAI 34
MAI 35
MCRD
MCWR
INT 21
-MAIX 19
MAIX 20
-MAIX 20
MAIX 21
-MAIX 21
INTX 35
-INTX 35
-MAI 19
MAI 20
-MAI 20
MAI 21
-MAI 21
-FMC SELECT
INT 35
-INT 35
-FMC SELECT
W851 CD31
W851 CD29
W851 CD21
W851 CD19
MAIX 18
-MAIX 18
MAIX 19
REQX CYC
-MAIX 22
MAI 18
-MAI 18
MAI 19
REQ CYC
-MAI 22
TO OF 10
ADDRACKX
RDRSX
ADDRACK
RDRS
TO MEM
MC PAR
MXC PAR
RDWR 2(1)
RDWR 1(0)
WRRS
IGNX PAR PULSE
WRRSX
IGN. PARITY PULSE
W021
D11
(SEE NOTE 4)
MCXRD FROM DEVICE
MCXWR FROM DEVICE
ADDRACK FROM MEM
RDRS FROM MEM
WRRSX FROM DEVICE
NOTES:
1. * NO INPUT CONNECTION NEED BE MADE TO THIS BOARD.
2. G70Ø TERMINATOR BOARDS ARE USED IN SPACES C21, C22, D21, D22, C31, C32, D31, D32 UNLESS EXTENSION CABLES FILL SAID SPACES.
3. UNUSED WIØ2 TRANSMITTER INPUT GATES IN C23 AND D23 ARE GROUNDED. (PINS M, R, AND U)
4. TEST CABLE SLOT USED WITH MX10 OFF-LINE TESTER

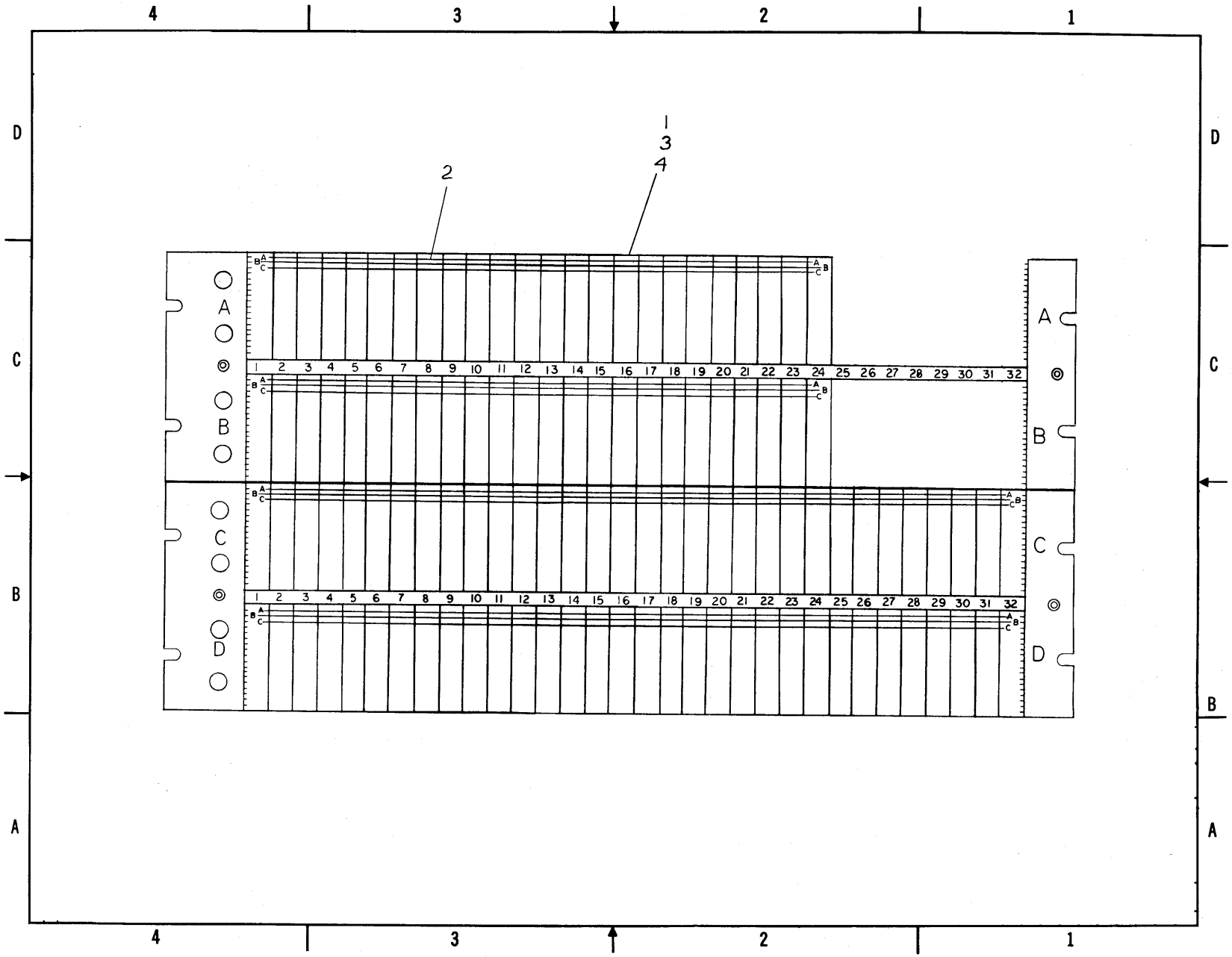


D-BD-MX10-0-4 Master Block Diagram

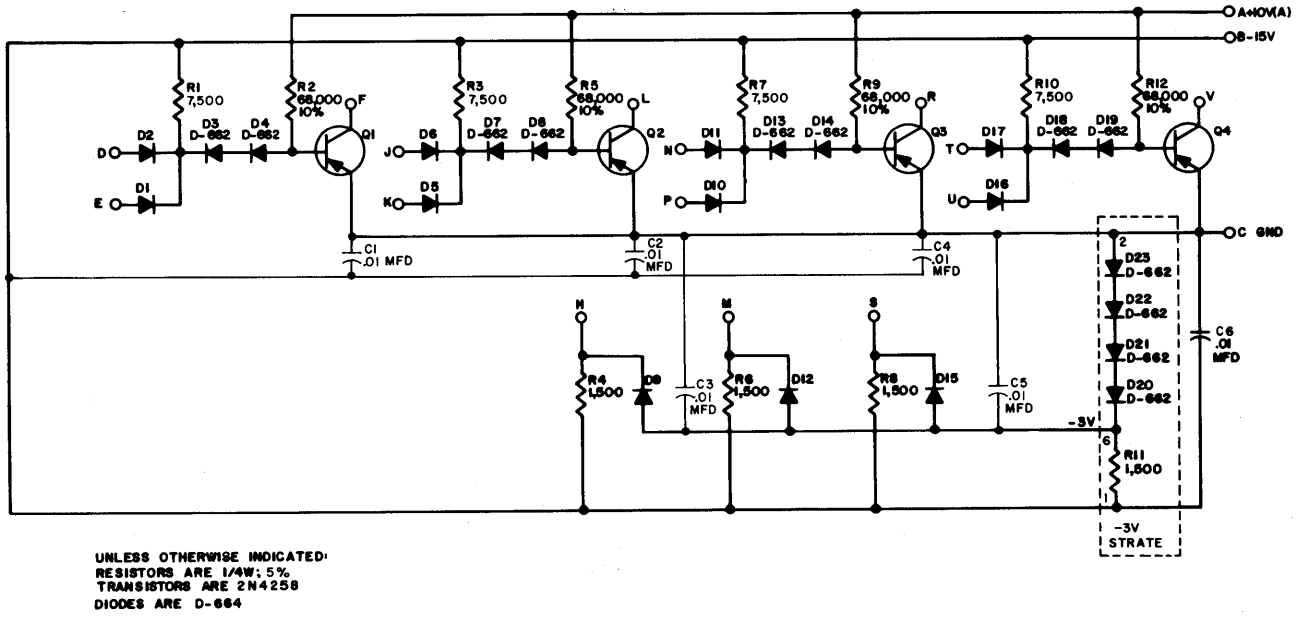


READ	WRITE	READ+WRITE
MCRD = 1	MCWR = 1	MCRD = 1
MCWR = Ø	MCRD = Ø	MCWR = 1

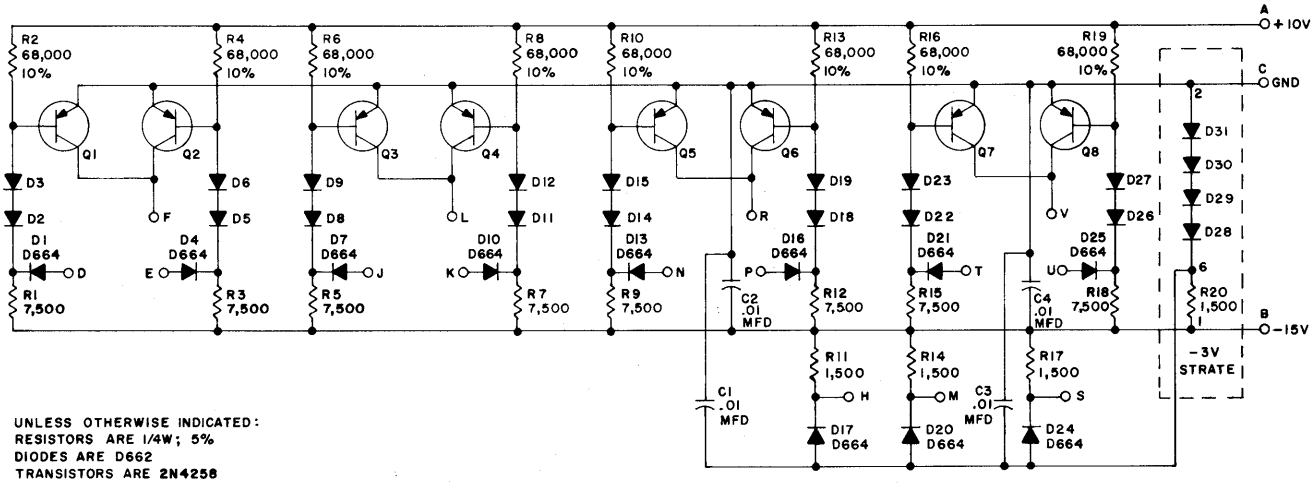

DISPLAY
PANEL
* NOTE: THIS SLOT USED FOR TEST CABLE WHICH CONNECTS TO MXIO OFF-LINE TESTER.



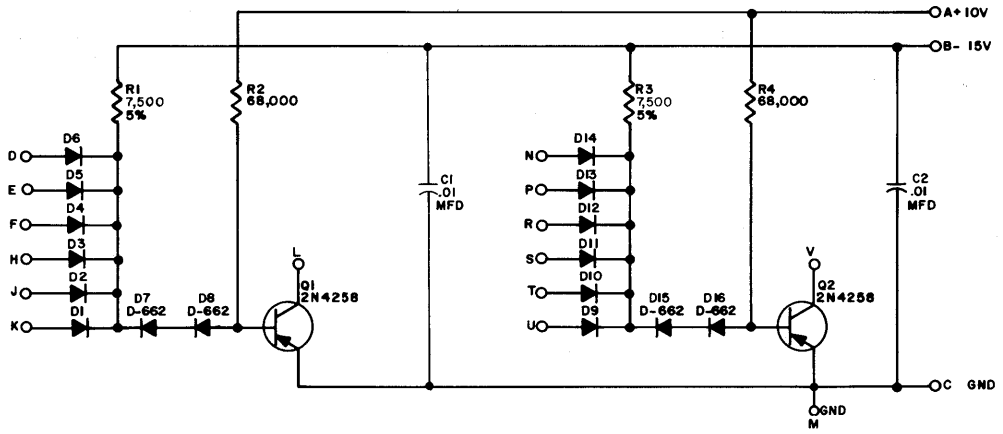
C-AD-7005509-0-0 Wired Assembly



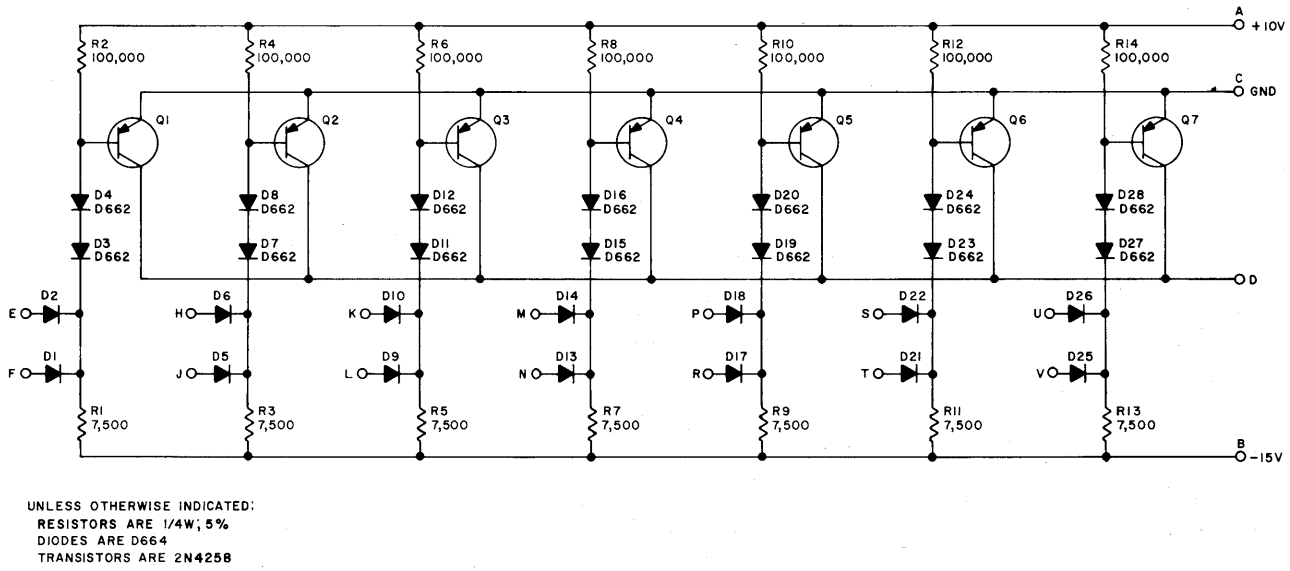
B-CS-B133-0-1 Diode Gate



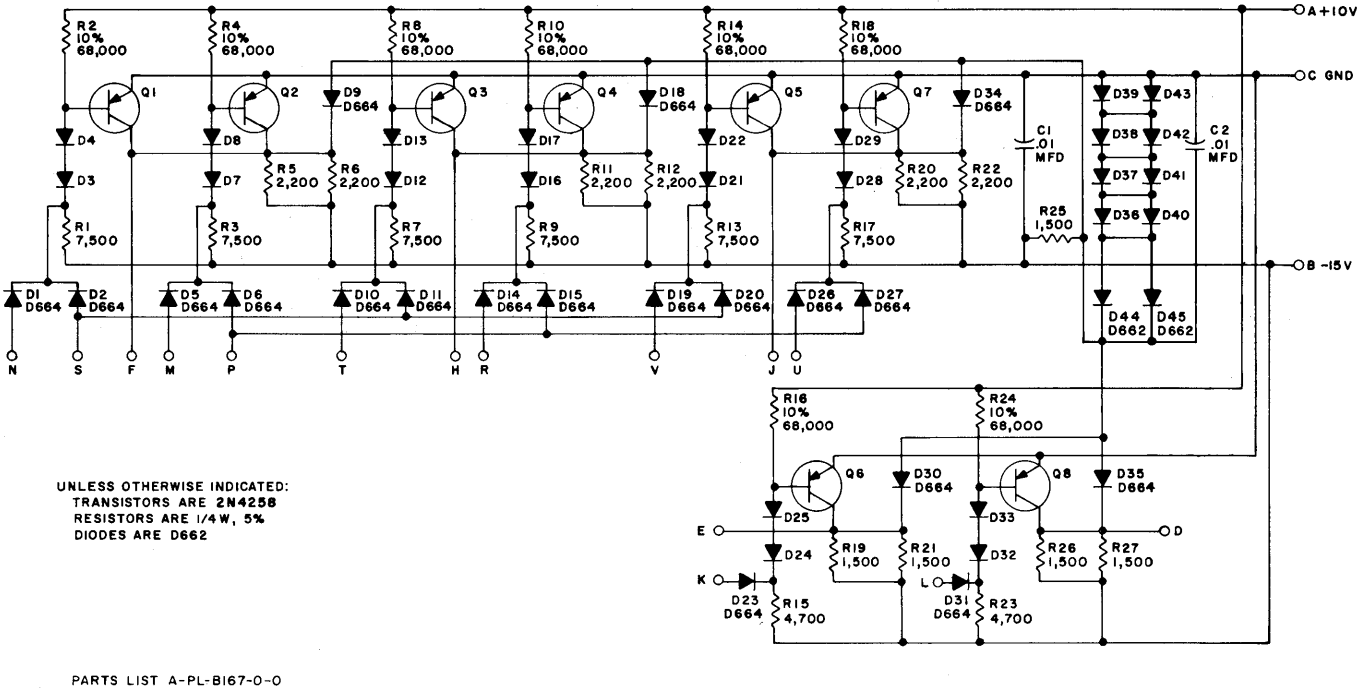
B-CS-B134-0-1 Diode Gate



B-CS-B137-0-1 Diode Gate



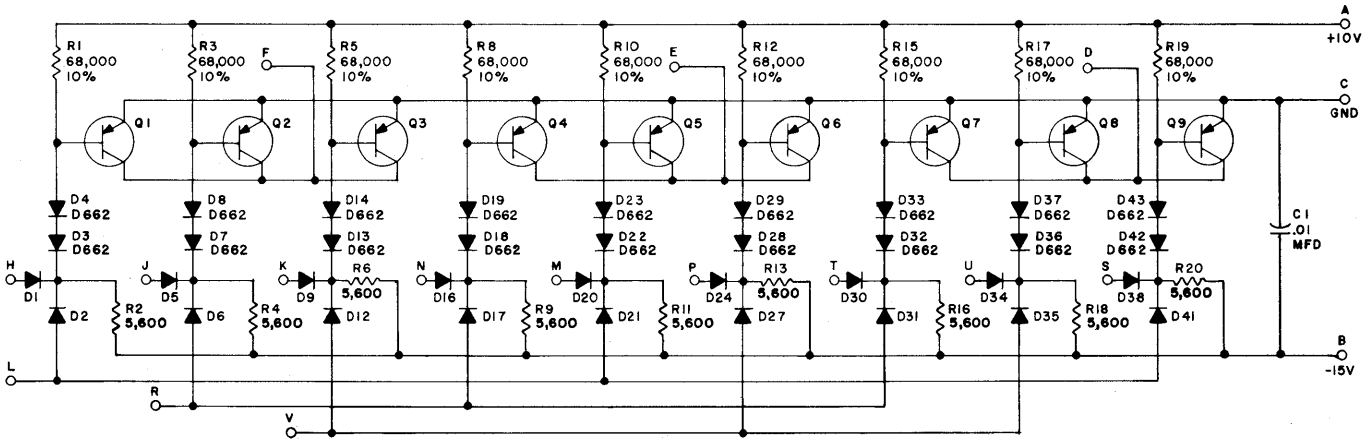
B-CS-B141-0-1 Diode Gate



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE 2N4258
RESISTORS ARE 1/4W, 5%
DIODES ARE D662

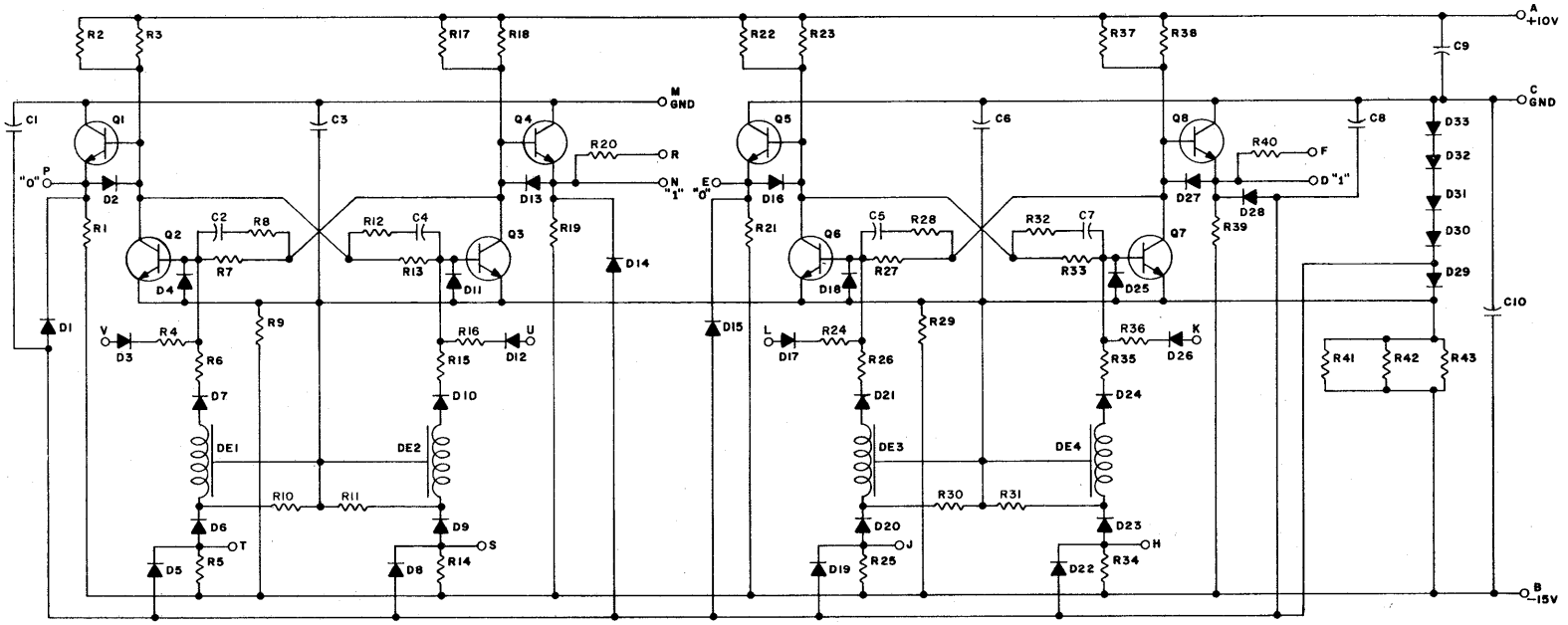
PARTS LIST A-PL-B167-0-0

B-CS-B167-0-1 Adder Gate

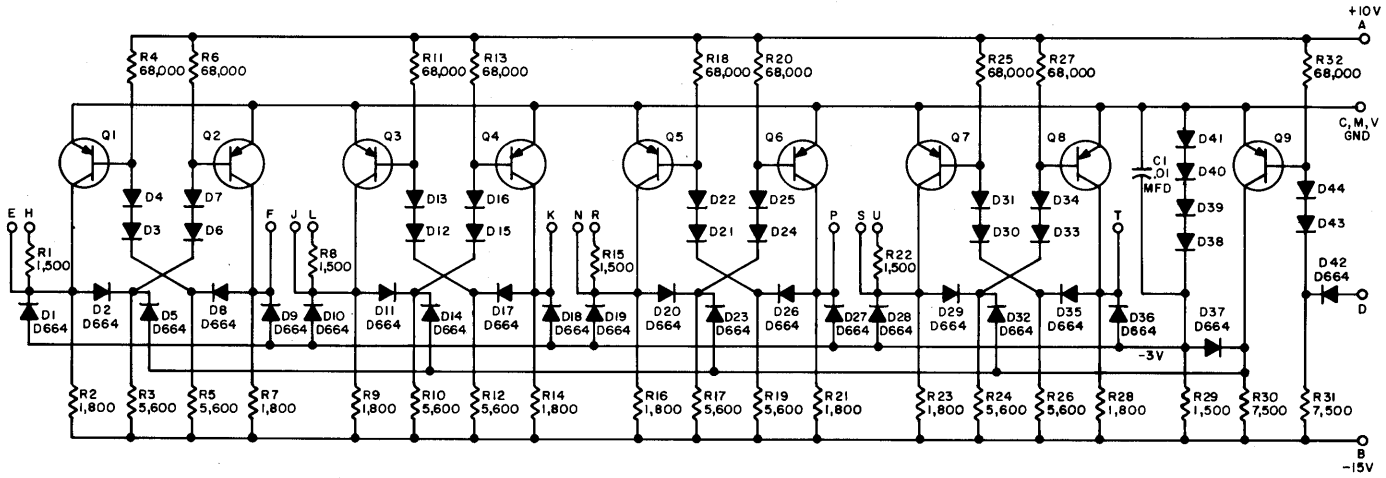


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D664
TRANSISTORS ARE 2N4258

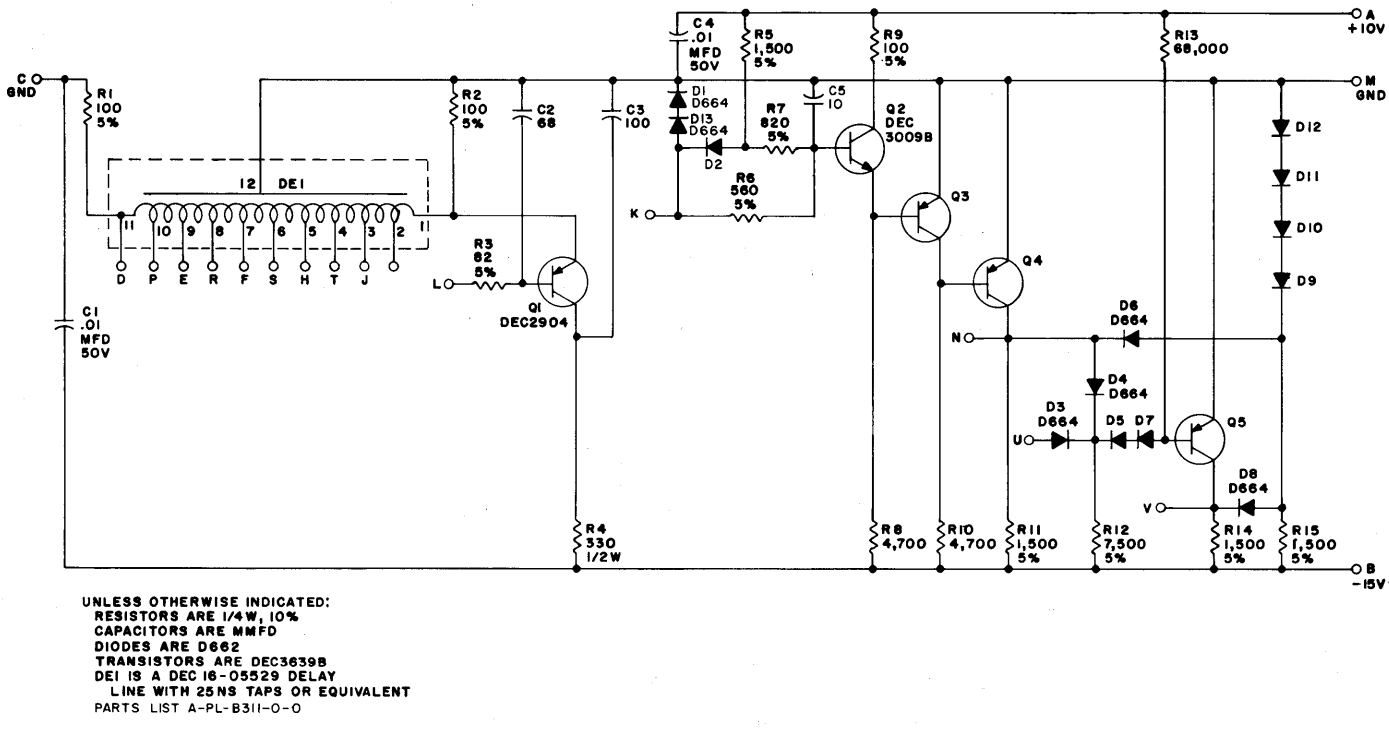
B-CS-B168-0-1 Diode Gate



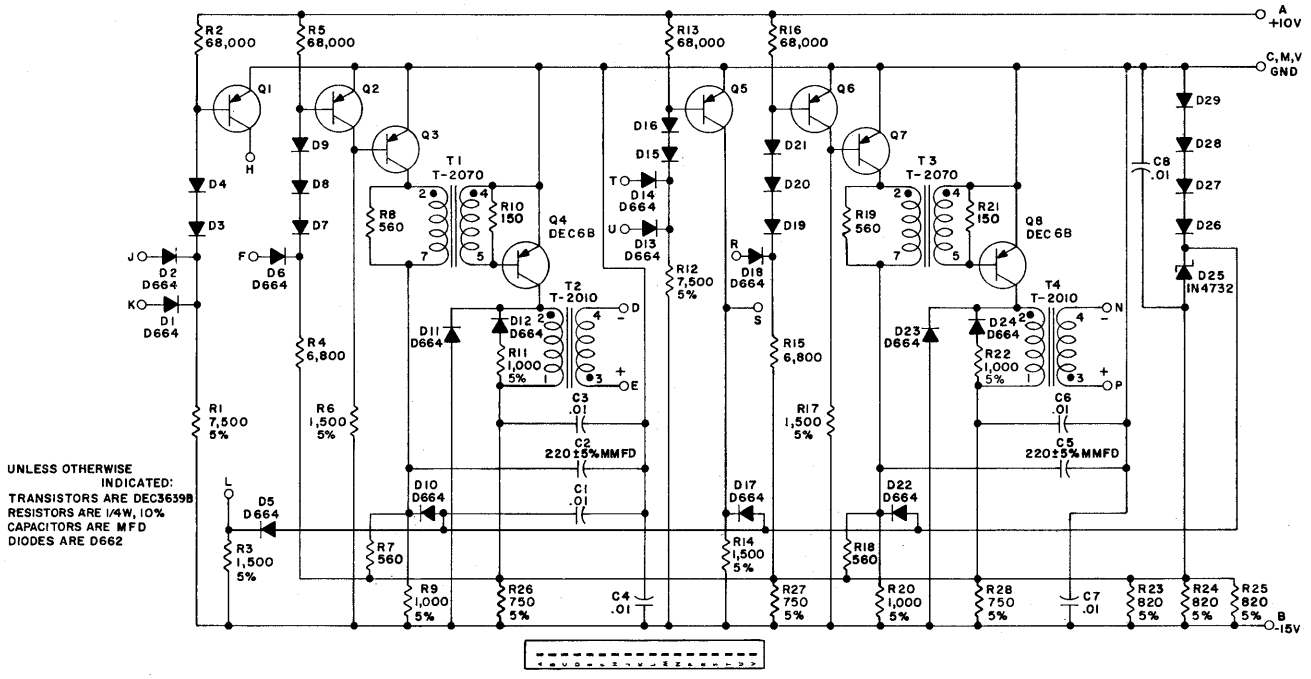
C-CS-B212-0-1 Flip-Flop



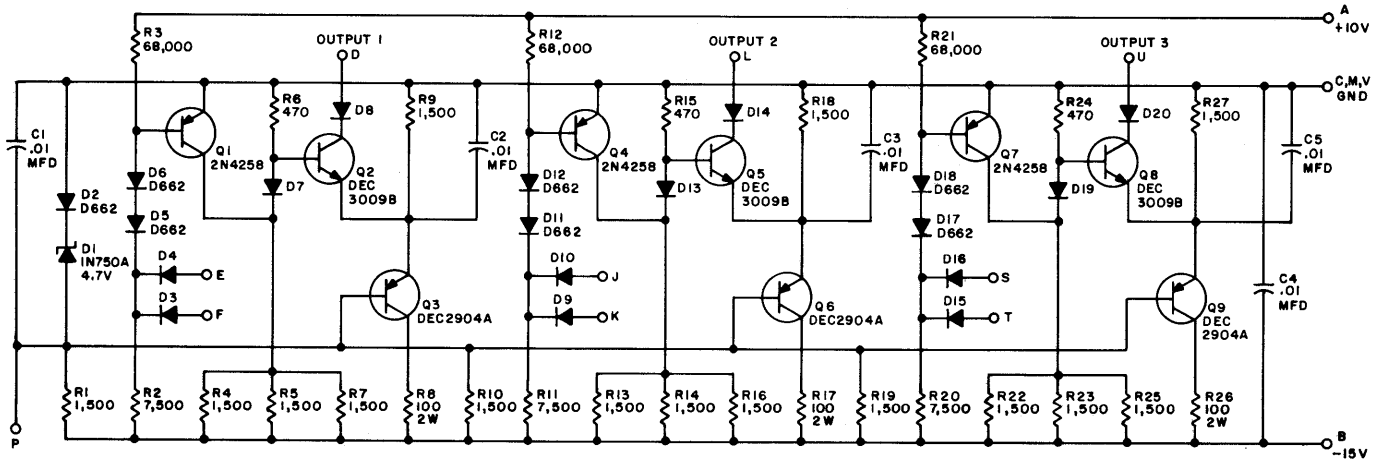
B-CS-B214-0-1 Quadruple Flip-Flop



B-CS-B311-0-1 Delay Line

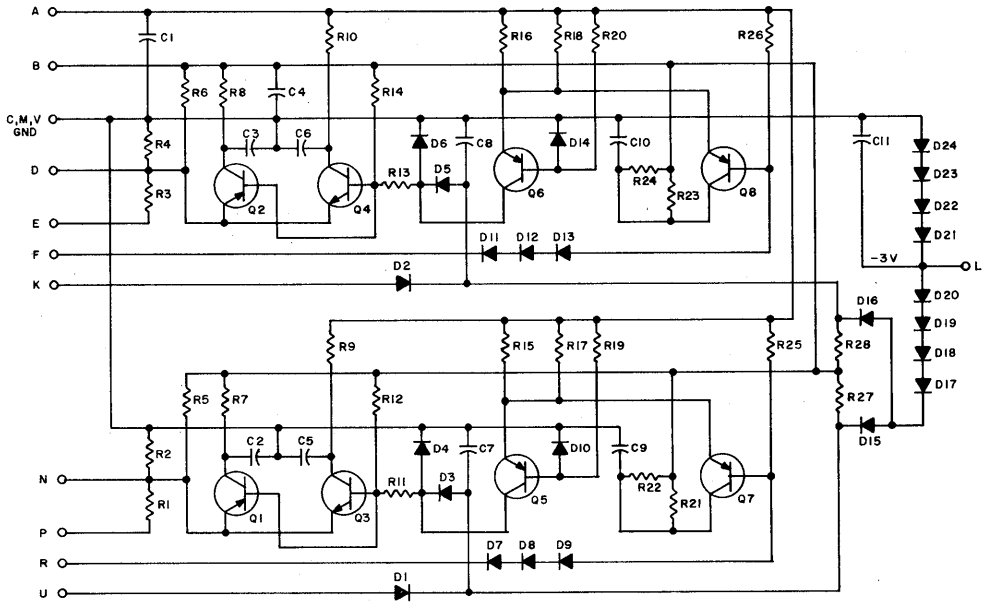


B-CS-B611-0-1 Pulse Amplifier

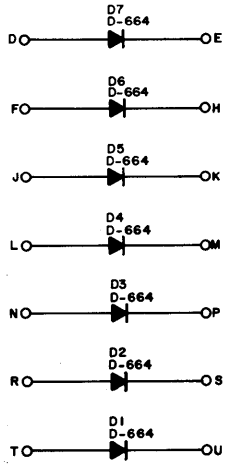


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D664

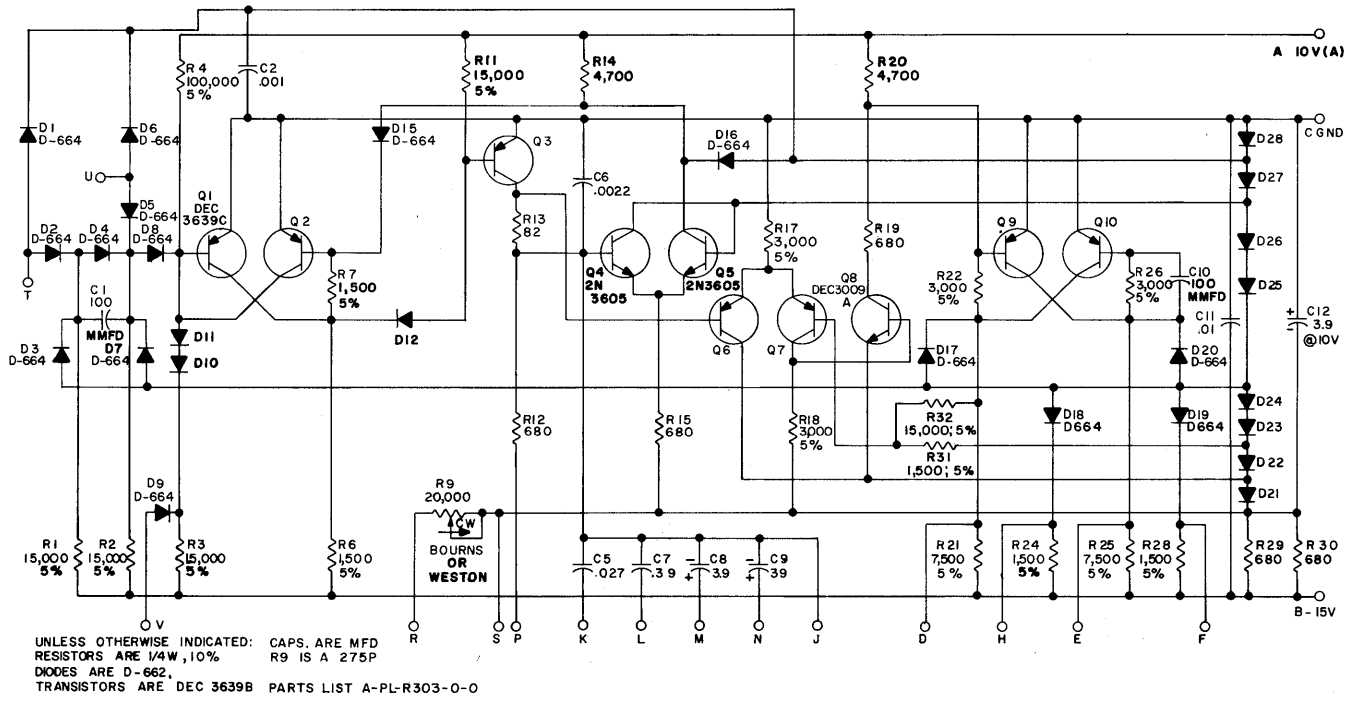
B-CS-B683-0-1 Bus Driver



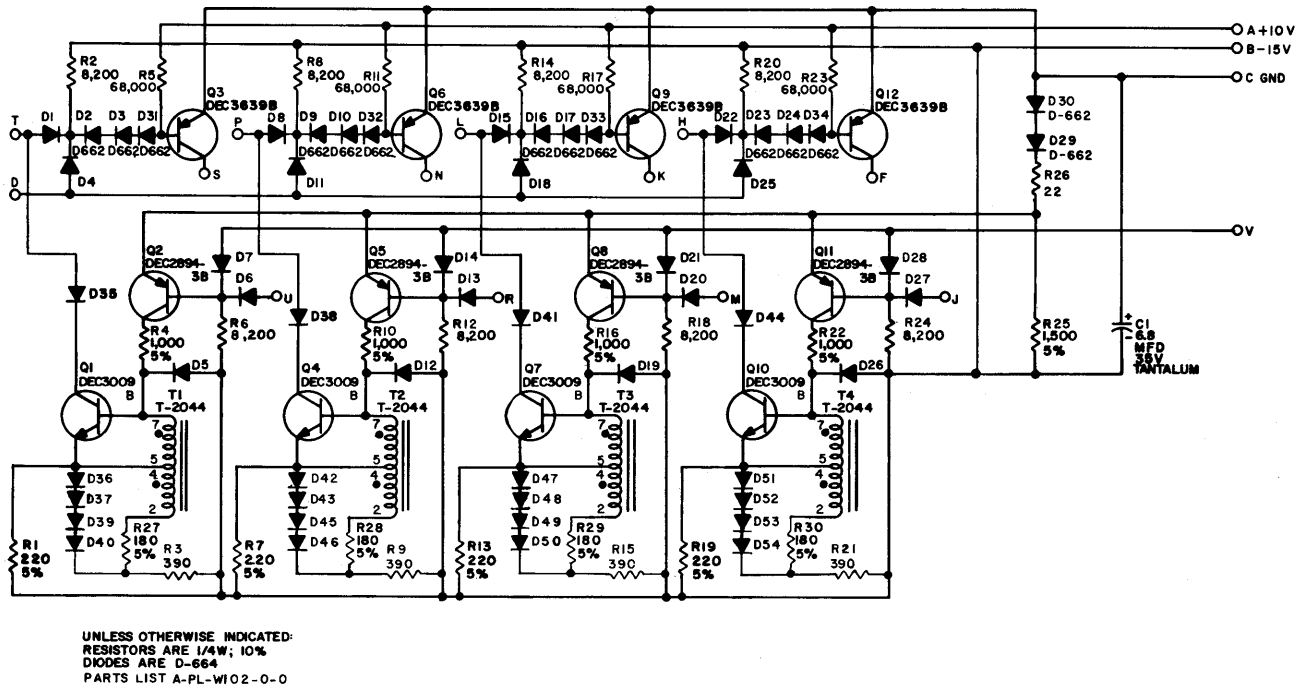
C-CS-B684-0-1 Bus Driver



B-CS-R001-0-1 Diode Network



B-CS-R303-0-1 Integrating One Shot



B-CS-W102-0-1 Pulsed Bus Transceiver

APPENDIX A

GLOSSARY

MNEMONICS - LEVELS - PULSES

ACK 0-7 (Acknowledge)	This level is placed on an MPX Control Line by the MX10 to signify to the Data Channel associated with that line that it has been granted access to the MX10.
ADDRACK (Address Acknowledge)	This pulse is developed in a memory unit and transmitted to the MX10 over the Memory Bus to signify that the memory address has been valid and that the memory unit is commencing its cycle.
ADDRACKX (Address Acknowledge MPX Bus)	This pulse is generated in the Bus Drivers and Control logic by ADDRACK and transmitted to the Data Channel being serviced, over the MPX Bus, to signify that the selected Data Channel has gained access to the memory unit and that the memory cycle is in progress.
BUSY	This flip-flop, located in the Control logic, when set, designates the MX10 BUSY state and, when cleared, designates the completion of a memory cycle.
BUSY DY (Busy Delayed)	This flip-flop, located in the Control logic, when set, fulfills one requirement for generation of an ACK level, thereby granting MX10 access to a requesting Data Channel.
CHN 0 - 7 (1) (Channel)	These levels are generated by setting the associated flip-flops CHN 0-7 located in the Control logic, and are tested in the priority selection network to determine which Data Channel will be granted access. Each flip-flop is set by a Data Channel requesting access while BUSY(0) is true.
CLR 0 - 7 (Clear)	A pulse generated in the selected Data Channel when a non-existent memory situation is detected.
FIN (Finish)	This pulse is generated in the Control logic by CLEAR and initiates the operations which place the MX10 in the ready condition.
FIN DY (Finish Delayed)	This pulse is derived from FIN (delayed 65 ns) and clears BUSY signifying the completion of a memory cycle.
HIACK (High Acknowledge)	This level is generated in the priority selection network of the Control logic and is an enabling condition for generation of ACK 4 - 7.
IGN PARITY PULSE (Ignore Parity Pulse)	This pulse is generated in a memory unit which does not have provisions for storing a parity bit and is transmitted to the MX10 over the Memory Bus.

IGNX PARITY PULSE (Ignore Parity Pulse MPX Bus)	This pulse is generated in the Bus Drivers and Control logic when IGN PARITY PULSE is asserted. Transmitted to the selected Data Channel over the MPX Bus, it causes the Data Channel INOR PAR indicator lamp to light and disables the parity checking network.
MCRD (Memory Cable READ)	This is the READ request level, developed in the Bus Drivers and Control logic from MCXRD. MCRD is transmitted to the memory unit over the Memory Bus.
MCWR (Memory Cable WRITE)	This is the WRITE request level, developed in the Bus Drivers and Control logic from MCXWR. MCWR is transmitted to the memory unit over the memory Bus.
MCXRD (Memory Cable MPX READ)	This is the READ request level developed in the selected Data Channel and transmitted to the MX10 over the MPX Bus.
MCXWR (Memory Cable MPX WRITE)	This is the WRITE request level developed in the selected Data Channel and transmitted to the MX10 over the MPX Bus.
RDRS (READ-Restart)	This pulse is generated in the memory unit and placed on the Memory Bus simultaneously with the data word read from core.
RDRS DY (READ-Restart Delayed)	This pulse is derived from RDRS and delayed 65 ns in the Control logic. RDRS DY causes RDWR1 and RDWR2 to be set to their 1 states thereby allowing MPX Bus to Memory Bus data transfers.
RDRSX (READ-Restart MPX Bus)	This is the pulse, triggered by RDRS, generated in the Bus Drivers and Control Logic that is transmitted to the selected Data Channel over the MPX Bus simultaneously with the data word read from core.
RDWR1 and RDWR2 (READ - WRITE)	These are the flip-flops, located in the Control logic, which, when in their 1 states, allow MPX Bus to Memory Bus data transfers, and, when in their 0 states, allow Memory Bus to MPX Bus data transfers.
REQ 0 - 7 (Request)	Each Data Channel requesting MX10 access places its associated REQ level on its REQ MPX Control Line.
REQ CYC (Request Cycle)	This is the level, triggered by REQX CYC in the Bus Drivers and Control logic which is placed on the Memory Bus simultaneously with the memory address word and which remains true until ADDRACK is generated by the memory unit.
REQX CYC (Request Cycle MPX Bus)	This is the level generated in the selected Data Channel after reception of the appropriate ACK level from the MX10. REQX CYC is placed on the MPX Bus simultaneously with the memory address word.

WR BUS (0) (WRITE Buffer)	This level is ANDed with RDRS DY in the Control logic to generate CLEAR at the completion of a memory READ cycle and, when false during a READ-MODIFY-WRITE cycle, prevents MX10 termination at the completion of memory READ.
WR BUF (1) (WRITE Buffer)	This level is ANDed with WRRS DY in the Control logic to generate CLEAR at the completion of a memory WRITE cycle.
WRRS (WRITE-Restart)	This is the pulse triggered by WRRSX in the Bus Drivers and Control logic which is transmitted to the selected memory unit over the Memory Bus simultaneously with the data word to be written into core.
WRRS DY (WRITE-Restart Delayed)	This is the pulse derived from WRRS and delayed 65 ns which, when ANDed with WR BUF (1) in the Control logic, causes generation of CLEAR.
WRRSX (WRITE-Restart MPX Bus)	This is the pulse generated in the selected Data Channel which is placed on the MPX Bus simultaneously with the data word to be written into core.

Digital Equipment Corporation
Maynard, Massachusetts

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